AN 8VSB SFN DISTRIBUTED TRANSLATOR SYSTEM

Steve Kuh
Ktech Telecommunications, Inc
Chatsworth, CA
www.ktechtelecom.com

This paper is to be presented at NAB 2010 - 64th Broadcast Engineering Conference

SYNOPSYS: An 8VSB Distributed (DTx) Translator System is introduced. Without using a GPS system, a DTx Translator is implemented in an SFN, where the input frequency is different than the output frequency. However, all of the DTx Translators are implemented with the same transmitting frequency. This allows a local DTV broadcaster to require only 1 channel for its entire translator system. However, the area of particular interest is this: What happens to an 8VSB signal reception when the DTx signals are overlapped between two or more DTx transmitters? The results indicate that the system performance is sensitive to symbol clock jitter in the main 8VSB transmitter. In addition, the proposed 8VSB SFN DTx translator would offer a wider coverage area than a system which is based on a GPS clock.

INTRODUCTION

When implementing a DTx system, the main technical challenge is the synchronization of carrier frequency and data among the multiple DTx Translators. The use of a GPS clock in an 8VSB DTx Translator system has been introduced in [1]. Slaving a local clock to the GPS clock as a common clock source, this system provides a synchronized DTx translated signal. However, GPS clock is only accurate on an average sense, e.g., over a day period. It jitters severely when viewed on a much shorter period of time, e.g., over several minutes. This is because a local GPS 10MHz clock is continuously updated to combat the effects of the atmosphere as the GPS satellites are passed across the sky.

The applicability of the DTx system in an on-channel booster has also been introduced in [2]. However, it is only a principle of physics that a large signal isolation must be maintained between the repeater output and its input in order for the on-channel booster to work. This system is inherently self-jamming, and must be implemented with extreme care. Under this condition, the on-channel booster allows DTV broadcaster to fill in the signal shadowed area. This may be an important technical solution for ATSC mobile applications to ensure continued signal coverage.

Another solution to an 8VSB DTx Translator system is an SFN based DTx translator, [3] [4]. Without using a GPS system, this system is implemented with phase-locked Oven Controlled Crystal Oscillator (OCXO) clocks and a frequency estimation technique to generate a synchronized DTx translated signal. The carrier frequency synchronization is achieved using a carrier offset extraction and its addition method. This technique is extended to symbol clock frequency as well. This system is not implemented with a Reed-Solomon FEC in its demodulator. Rather, it takes the demodulated symbols from a specialized equalizer design and directly modulates to 8VSB, bypassing RS decoder/encoder. While this suffers a bit error degradation for the input, additional steps are taken in the equalizer to perform Trellis Decoder with Trace Back Depth of 1 in order to gain some error rate improvement, [4].

In this paper, an 8VSB SFN DTx Translator system is introduced. An input carrier frequency is different than the output carrier frequency. This way, physical signal isolation is not required between the output and the input of the DTx Translator. However, all of the output frequencies of the DTx system are the same. This way, only 1 RF channel is required to implement the SFN 8VSB DTx Translator system. This system also offers a good solution to expand signal coverage and fill-in the signal shadowed areas for an improved ATSC mobile system.

AN 8VSB SFN DTx TRANSLATOR

A system block diagram of the 8VSB SFN DTx Translator is shown in Figure 1. The input is an 8VSB RF signal. After a Band-Pass Filter (BPF) and a Low-Noise-Amplifier (LNA), the resulting signal is further down-converted, sampled, demodulated, processed, modulated, and up-converted to an output frequency in the 8VSB DTx Exciter. The RF output signal from the exciter is amplified, filtered, and transmitted. The input carrier frequency is different than the output carrier frequency. Note that there is no use of a GPS system to provide a reference clock for the exciter. All system clocks are derived from an input 8VSB signal.

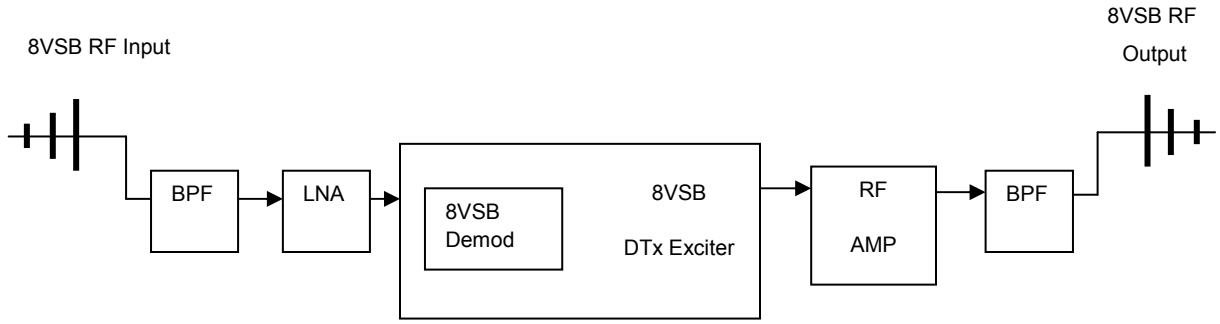

Figure 1 System Block Diagram of an 8VSB SFN DTx Translator

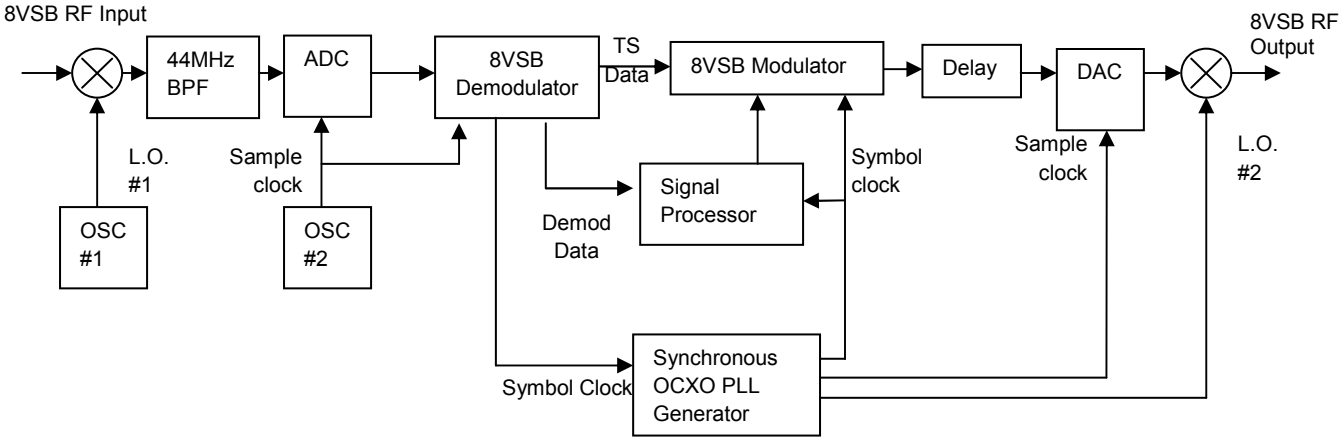

Figure 2 Details of the 8VSB SFN DTx Exciter

The Details of the 8VSB SFN DTx Exciter is shown in Figure 2. Without using a GPS locked clock, all of the transmitting clocks are generated based on phase-locked clocks that are slaved to a demodulated 8VSB symbol clock. It is also possible to achieve the same performance by using other equivalent clocks that are phase-locked to the demodulated 8VSB symbol clocks such as a demodulated Transport Stream clock, a Reed-Solomon Byte clock, and a Field Sync Clock. A full and complete 8VSB demodulation is performed in the 8VSB demodulator including Reed-Solomon Error Correction decoding and Trellis Decoding. This is done so that the system can take advantage of the error correction capability of the Reed-Solomon Decoding and Trellis Decoding. The resulting decoded signal is re-modulated using ATSC A53 8VSB modulation standard, except that the contents of the Trellis Encoder is controlled using a memory initialization algorithm.

Furthermore, a variable time delay is introduced at the output of the 8VSB modulator in order to facilitate a system adjustment during initial set up, and, therefore, will allow a signal time delay on the output of the DTx Translator. This time delay can be set in accordance with the system requirement such that the signal overlapped area will be presented with a minimum multi-path signal distortion (i.e., short signal echo delay easily within consumer product equalizer delay ranges). Since all of the DTx transmitting signals are locked in frequency and symbols of the main 8VSB signal, the receiving 8VSB consumer Set-Top-Box (STB) or digital television (DTV) set will treat the signals arriving from different DTx Translators as if it is receiving a multi-path distorted signal. Thus, the system delay parameters can be set based on geographical location of the DTx translators and its estimated signal overlapped area for a minimal signal multi-path distortion.

In addition to the delay parameter of the DTx Translator, the system requires a method of initializing the Trellis Encoder memory. Because of the infinite memory nature of the Trellis Encoder, as shown in Figure 3, in the 8VSB modulator, it is important to reinitialize the memory states of the Trellis Encoder in the DTx Translator in a synchronized way. This is especially important since individual DTx Translators may start up at a different time due to loss of power or a manual reset by an operator.

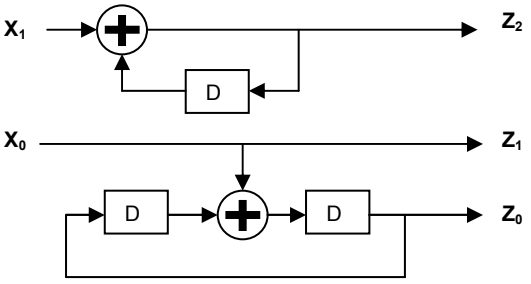

Figure 3 Trellis Encoder Memory

There are many ways to initialize the Trellis Encoder memory. One of the ways is to simply reset the contents of the memory of the Trellis Encoder to a fixed known state in a periodic interval of time, e.g., every frame at 48.4 mSec, [5]. It has been reported that a fraction of dB SNR loss can result due to the simple memory reset technique.

The fixed known state could be all zeros, all ones, or any other predetermined state. While this is a simple technique, this will cause packet errors in the receiver every time the Trellis Encoder memory is reset. However, it is most likely that the errors are corrected by the error correction mechanism built in a receiving consumer 8VSB STB. Resetting of the Trellis Encoder memory to a periodic and fixed known state will cause a bit error rate degradation.

Another way to reinitialize the Trellis Encoder memory of the 8VSB modulator in the DTx Exciter is to recalculate the contents of the Trellis Encoder based on the incoming demodulated data. By knowing exact data from the 8VSB demodulator without any modifications such as null packet insertions or deletions, the contents of the Trellis Encoder memory can be recalculated by processing through Randomization, Interleaving, and Trellis Encoding. This way, all symbols are formulated the same way in all of the DTx Translators. Therefore, all of the 8VSB data symbols are exactly matched.

A suitable framing signal is obtained from the 8VSB demodulator as a reference frame time signal for the 8VSB modulator in the DTx Exciter. In this case, a recovered frame sync signal from the 8VSB demodulator is used. However, there can be other suitable framing signals that could be used such as recovered RS clocks or recovered Interleaver clocks from the 8VSB Demodulator.

As for the synchronization of the transmit carrier frequency in the DTx Translator, no GPS related clocks are used. All of the transmitting clocks are generated based on phase-locked OCXO clocks which are slaved to a recovered 8VSB symbol clock or its equivalently phase-locked clocks such as a demodulator transport stream clock. Since all of the DTx Translators are phase-locked to the main 8VSB transmitter signal, no GPS based common reference is needed. There is no other signal processing used to estimate the carrier frequency or phase and apply the estimation to the transmit carrier phase or to the transmit clocks. No carrier frequency extraction and its addition are necessary.

PERFORMANCE RESULTS

In order to measure the system performance, test hardware has been implemented as shown in Figure 4. A Segment Error Rate (SER) is used as a performance metric.

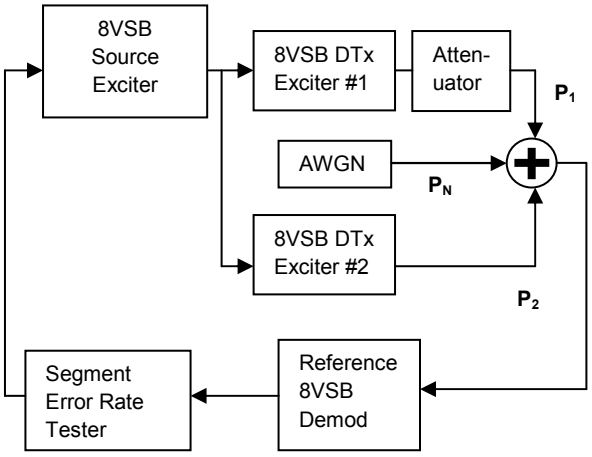

Figure 4 Hardware System Block Diagram

An average Segment Error Rate was measured over 5 minutes for all SER points. As for the reference 8VSB demodulator, an LGDT3304 6th generation 8VSB demodulator IC is used in the reference 8VSB Demodulator to obtain all of the SER results. The reference 8VSB demodulator block also contains a Band-Pass-Filter, an LNA in its front-end, and an RF tuner. By employing an RF attenuator on the output of the DTx Exciter #1, the test hardware can show performance of varying power ratio between the DTx Exciters.

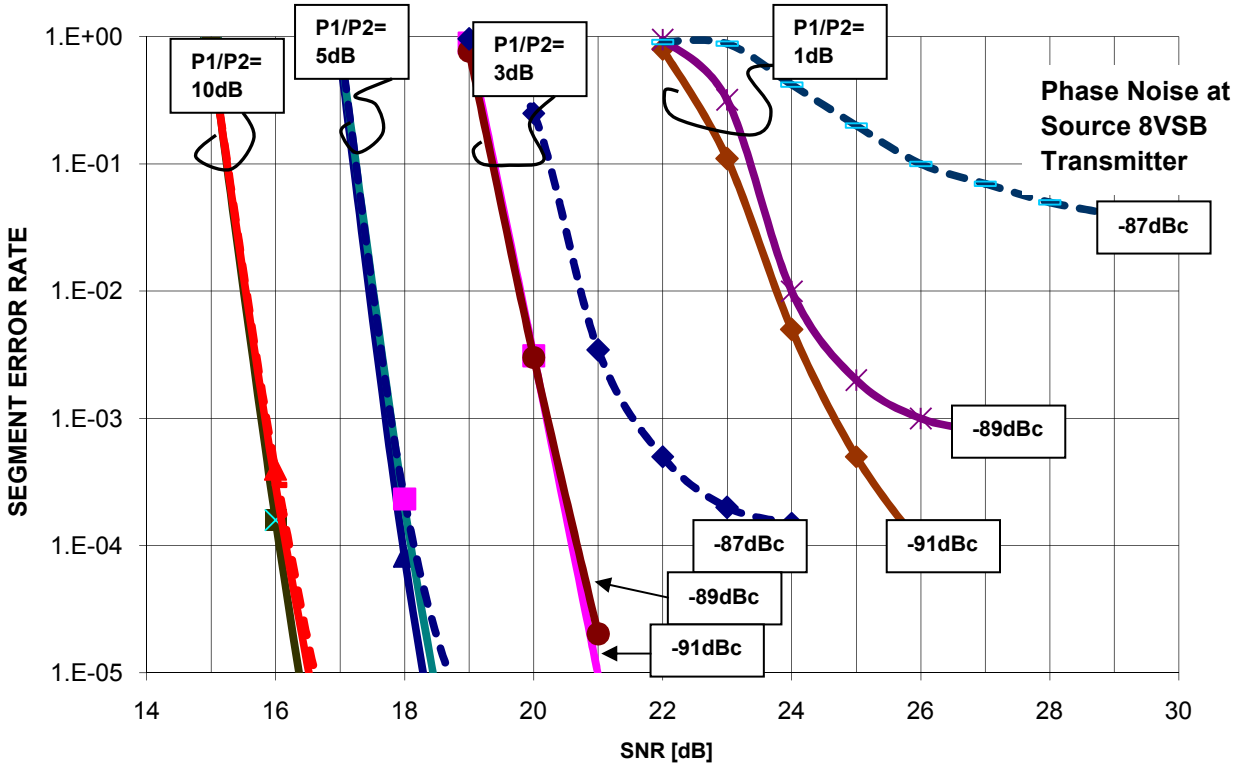

Figure 5 SER vs SNR at 1uSec Delay at –87dBc, -89dBc, and -91dBc @ 10KHz Source Symbol Clock Phase Noise

The signal power output from the DTx Exciter #1 is defined as P1 and Exciter #2 as P2. The time delay between the DTx #1 and #2 is also varied. The SNR is defined as a ratio of P_S/P_N, where P_S is measured over a 6MHz equivalent noise bandwidth for the combined signal power of P1 and P2 and where P_N is measured over a 6MHz equivalent noise bandwidth for the AWGN noise signal.

In the case of the DTx Translator system, it has been found that the SER performance is sensitive to symbol clock phase noise in the 8VSB Source Exciter. This is characterized in Figures 5 for the source symbol clock phase noise of -87dBc, -89dBc, and -91dBc, respectively, at 10KHz offset. This phase noise was measured on an 86.0979MHz clock that was running at 8 times the symbol rate in the 8VSB Source Exciter.

Based on SER results in Figures 5, it is interesting to note that higher SNR is needed for a given SER as the power difference between the DTx #1 and #2 becomes closer to each other. That is, there is more multipath-induced equalizer noise enhancement in the receiver when the two synchronized signals are closer to each other in terms of signal level. From Figure 5, it can be seen that, for 1E-4 SER, a DTx signal overlapping coverage area where the two DTx signals arrive with 1 uSec of time delay with each other and 1 dB power difference will require as much as 10 dB more power relative to the case that presents a received signal power difference of 10 dB between DTx #1 and #2.

Receiving a DTx signal power that is close to each other is a very realistic scenario when the signal coverage of the DTx Translators is overlapped. Typically, this may present an equal power at the worse case, i.e. the signal power received from DTx #1 is the same as the signal power received from DTx #2. Note that an overlapping 8VSB signal coverage with the DTx power ratio at 1dB is possible using this 8VSB SFN DTx Translator technique.

Based on SER results in Figures 5, it is not surprising to see that the SER performance becomes worse as the clock jitter in the main source 8VSB is increased. In fact, at –87dBc source symbol clock phase noise, the SER shows that it actually flattens out as SNR is increased for all power ratios of P1/P2. This is indicative of the fact that the jitter in the source 8VSB symbol clock starts to dominate the system SER performance in a DTx Translator system.

Realizing that the only clock jitter specification on ATSC 8VSB transmission system is the SMPTE-310M

that defines 19.39Mbps transport stream clock jitter, this may need to be revisited and refined for the DTx Translator application.

Figure 6 shows the SER performance of the DTx Translators when the system is phase-locked to GPS 10MHZ sources. Two Trimble Thurderbolt E GPS Disciplined Clocks are used to synchronize the two DTx Translators. One GPS antenna was intentionally located at one side of a building, and another GPS antenna was located on the other side of a building to ensure that the two GPS receivers are seeing different sets of the GPS satellites. As for the source 8VSB Transmitter clock phase noise, no clock jitter was introduced.

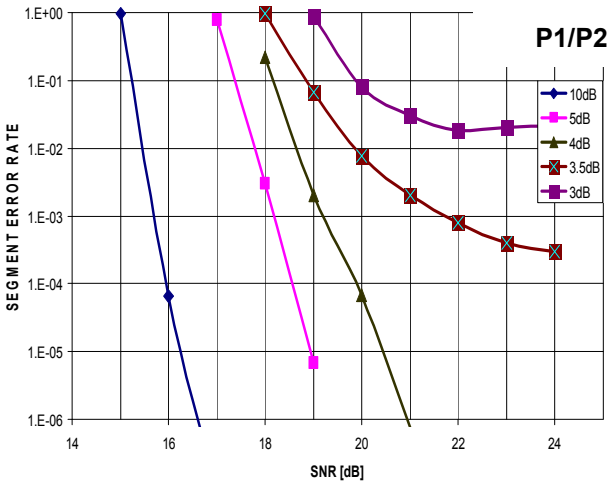

Figure 6 DTx Translator SER with GPS

As can be seen above in Figure 6, the use of GPS clock as means to slave multiple DTx Translators will work fine for the DTx receiving signal power ratios of 4 dB or higher. However, other power ratios of less than 4 dB show that SER performance degrades severely when the GPS system is employed in the DTx System. It is reasoned that the GPS 10MHz reference clocks are continuously updated for the atmospheric effects as the satellites are passed across the sky. This clock update occurs at all times and results in a performance degrading clock jitter as it is used in the DTx Translator system. It also means that DTx Translators based on GPS system will offer far less coverage area for an overlapping 8VSB signal area in an SFN distributed 8VSB transmission system. For an ATSC mobile application, any coverage gap is a critical system service issue. This can be overcome with the proposed 8VSB SFN DTx Translator System.

Figure 7 shows the Segment Error Rate against SNR for the case of resetting the Trellis Encoder memory (RESET as shown) and the case that recalculates the Trellis Encoder memory (NO RESET as shown) using 2 DTx system and 1uSec of time delay between them. The dotted lines are NO RESET case, and the solid lines are RESET case. It shows that there is about 0.1~0.2dB of SNR improvement for the NO RESET case.

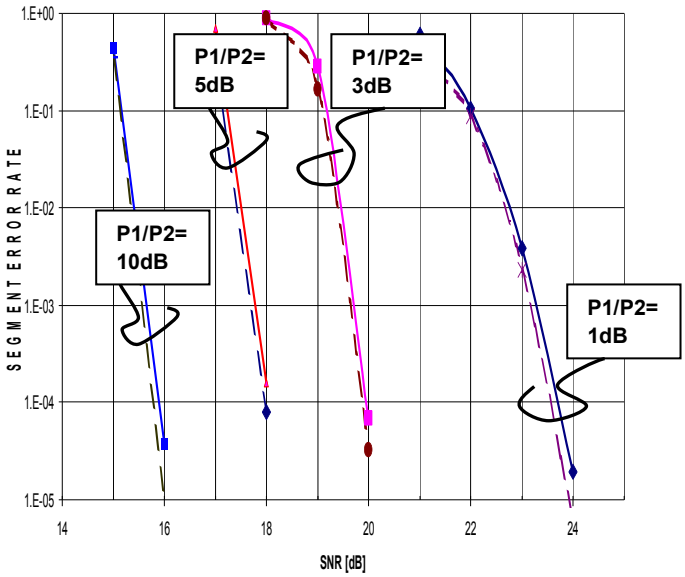

Figure 7 DTx Translator SER for Trellis Encoder Memory Reset and No Reset with 1uSec Delay

CONCLUSIONS

An 8VSB SFN DTx Translator System has been proposed. This system employs a combination of OCXO phase-locked clocks that are synchronized to a recovered 8VSB symbol clock and an estimation of Trellis Encoder memory in the DTx Translator Exciter. Through measurement of test hardware, Segment Error Rate results indicate that the DTx system is sensitive to a clock jitter in the source 8VSB transmitter. The current ATSC specification for the 8VSB symbol clock jitter may have been acceptable for a single transmission system. However, for a distributed transmission of 8VSB in an SFN, it has been found that the symbol clock jitter in the main source 8VSB transmitter has a major influence on the performance of the DTx Translators.

It is also concluded that the use of GPS as means to synchronize DTx Translators may have a limited performance. In fact, the proposed 8VSB SFN DTx Translator may offer a wider signal coverage. More studies are recommended to determine the jitter

performance and the sensitivity of DTx Translators to the source 8VSB transmitter symbol clock jitter.

ACKNOWLEDGEMENTS

The author wishes to acknowledge the works of Eric Jiang in implementing the hardware and obtaining the Error Rate performance results presented in this paper. The author also wishes to thank Gary Sgrignoli for his helpful comments and insights in reviewing of this paper.

REFERENCES:

[1] ATSC, "A/110B: Synchronization Standard for Distributed Transmission, Revision B", Advanced Television Systems Committee, Washington, D.C., December 2007

[2] S. Kuh, "Digital On-Channel Booster for 8VSB" 53rd Annual IEEE Broadcast Symposium, Washington D.C., Oct 2003

[3] H. Eum et al, "Frequency Synchronization among Translators for DTV Broadcasting Network", 59th Annual IEEE Broadcast Symposium", Alexandria, VA, Oct 2009

[4] H.Kim et al, "Field Test Results of Equalization Distributed Translators", 59th Annual IEEE Broadcast Symposium", Alexandria, VA, Oct 2009

[5] Y.W. Suh et al, "A Novel Data Synchronization Method for ATSC Distributed Translator", 20th Annual IEEE International Symposium on Personal, Indoor and Mobile Radio Communications, Tokyo, Japan Sept. 2009