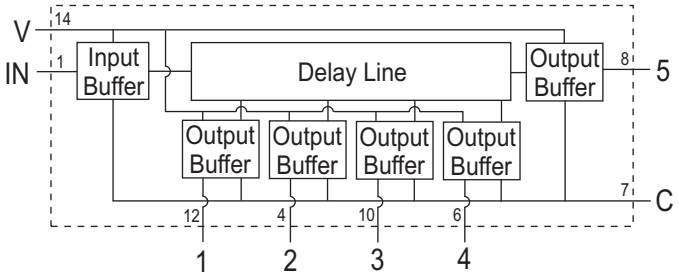
Surface Mount CMOS Logic Delay Module

The Surface Mount CMOS Logic Delay Modules manufactured by Engineered Components Company are designed to provide output waveforms that reproduce the input waveform after a set amount of delay time has elapsed. The five output waveforms are delay line taps provided at 20% increments of the total delay (20, 40, 60, 80, and 100%). These delay modules are non-inverting. The delay times are calibrated to the listed tolerances on the rising edge delays. The products with a total delay of less than 75ns have additional delay present at tap 1 due to internal propagation delays (see the Product Selection Table).

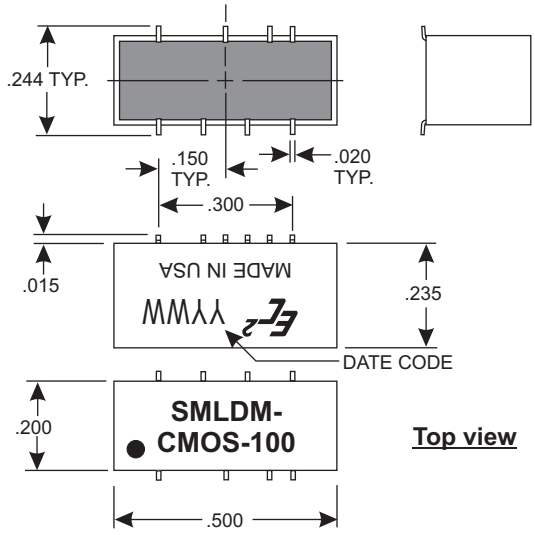
The MTBF on these modules, when calculated per MIL-HDBK-217, for a 50 deg.C ground fixed environment and with 50VDC applied, is in excess of 3 million hours. The temperature coefficient of delay is less than 500 ppm/deg.C over the operating temperature range of -40 to +85 deg. C.

The module is provided in a SO-14 package, fully encapsulated in epoxy resin and is housed in a Diallyl Phthalate case, blue in color. The case marking is applied by silkscreen using white epoxy paint. The 8 beryllium copper leads are tin-lead plated and meet the solderability requirements of MIL-STD-202, Method 208.

BLOCK DIAGRAM



MECHANICAL DIAGRAM



Top view

Product Selection Table

Part Number	Output Delay and Tolerances (in ns)				
	Tap 1 (20%)	Tap 2 (40%)	Tap 3 (60%)	Tap 4 (80%)	Tap 5 (100%)
SMLDM-CMOS-26	16.0+/-1.0	18.5+/-1.0	21.0+/-1.0	23.5+/-1.0	26.0+/-1.0
SMLDM-CMOS-28	16.0+/-1.0	19.0+/-1.0	22.0+/-1.0	25.0+/-1.0	28.0+/-1.0
SMLDM-CMOS-32	16.0+/-1.0	20.0+/-1.0	24.0+/-1.0	28.0+/-1.0	32.0+/-1.0
SMLDM-CMOS-35	15.0+/-1.0	20.0+/-1.0	24.0+/-1.0	30.0+/-1.5	35.0+/-1.5
SMLDM-CMOS-39	15.0+/-1.0	21.0+/-1.0	27.0+/-1.5	33.0+/-1.5	39.0+/-1.5
SMLDM-CMOS-43	15.0+/-1.0	22.0+/-1.0	29.0+/-1.5	36.0+/-1.5	43.0+/-1.5
SMLDM-CMOS-47	15.0+/-1.0	23.0+/-1.0	31.0+/-1.5	39.0+/-1.5	47.0+/-1.5
SMLDM-CMOS-51	15.0+/-1.0	24.0+/-1.0	33.0+/-1.5	42.0+/-1.5	51.0+/-2.0
SMLDM-CMOS-55	15.0+/-1.0	25.0+/-1.0	35.0+/-1.5	45.0+/-2.0	55.0+/-2.0
SMLDM-CMOS-59	15.0+/-1.0	26.0+/-1.0	37.0+/-1.5	48.0+/-2.0	59.0+/-2.0
SMLDM-CMOS-63	15.0+/-1.0	27.0+/-1.0	39.0+/-1.5	51.0+/-2.0	63.0+/-2.5
SMLDM-CMOS-67	15.0+/-1.0	28.0+/-1.5	41.0+/-1.5	54.0+/-2.0	67.0+/-2.5
SMLDM-CMOS-71	15.0+/-1.0	29.0+/-1.5	43.0+/-1.5	57.0+/-2.0	71.0+/-2.5
SMLDM-CMOS-75	15.0+/-1.0	30.0+/-1.5	45.0+/-2.0	60.0+/-2.5	75.0+/-2.5
SMLDM-CMOS-80	16.0+/-1.0	32.0+/-1.5	48.0+/-2.0	64.0+/-2.5	80.0+/-3.0
SMLDM-CMOS-85	17.0+/-1.0	34.0+/-1.5	51.0+/-2.0	68.0+/-2.5	85.0+/-3.0
SMLDM-CMOS-90	18.0+/-1.0	36.0+/-1.5	54.0+/-2.0	72.0+/-2.5	90.0+/-3.0
SMLDM-CMOS-95	19.0+/-1.0	38.0+/-1.5	57.0+/-2.0	76.0+/-2.5	95.0+/-30
SMLDM-CMOS-100	20.0+/-1.0	40.0+/-1.5	60.0+/-2.0	80.0+/-3.0	100.0+/-3.0
SMLDM-CMOS-125	25.0+/-1.0	50.0+/-2.0	75.0+/-2.5	100.0+/-3.0	125.0+/-4.0
SMLDM-CMOS-150	30.0+/-1.5	60.0+/-2.0	90.0+/-3.0	120.0+/-4.0	150.0+/-5.0
SMLDM-CMOS-175	35.0+/-1.5	70.0+/-2.5	105.0+/-4.0	140.0+/-5.0	175.0+/-5.0
SMLDM-CMOS-200	40.0+/-1.5	80.0+/-3.0	120.0+/-4.0	160.0+/-5.0	200.0+/-6.0
SMLDM-CMOS-225	45.0+/-2.0	90.0+/-3.0	135.0+/-4.0	180.0+/-6.0	225.0+/-7.0
SMLDM-CMOS-250	50.0+/-2.0	100.0+/-3.0	150.0+/-5.0	200.0+/-6.0	250.0+/-8.0

Special modules can often be manufactured to provide for customer specific applications.

Operating Specifications:

All measurements made at 25 deg. C
All measurements made with Vcc = +5VDC
All measurements made with (1) CMOS output load

Operating Temperature: -40 to +85 deg. C
Storage Temperature: -55 to +125 deg. C

Vcc Supply Voltage: 4.5 to 5.5VDC
Vcc Supply Current:
  Constant "0" in = 10mA typical
  Constant "1" in = 0.1uA typical
Logic "High" Input:
  Voltage: 2.0VDC min. ; 5.5VDC max.
  Current: 2.4VDC = 0.1 max.
Logic "Low" Input:
  Voltage: 0.8 VDC max.
  Current: 0.1uA max.
Logic "High" Voltage Out: 3.84VDC min.
Logic "Low" Voltage Out: 0.33VDC max.

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