3-Bit Trimmable Analog Delay Line

The 3-Bit Trimmable Analog Delay Lines manufactured by Engineered Components Company are designed to provide precise and stable delays for analog delay line applications. These are longer delay lines with digitally trimmable steps selected by the presence of either a TTL "high" or a TTL "low" at each programming pin to allow for final delay adjustment during or after installation in a circuit. Trimming may be accomplished in 8 equal delay steps by remote switching or by permanent termination of the appropriate programming pins. Vcc (+5V typical) and Vee (-5V typical) are required for proper operation of the digital controls. The enable pin should be connected to a TTL "low" during normal operation. When the enable pin is high, the outputs are disabled to a high impedance "off" state.

The MTBF on these delay lines, when calculated per MIL-HDBK-217, for a 50 deg.C ground fixed environment and with 50VDC applied, is in excess of 1.5 million hours. The temperature coefficient of delay is less than 100 ppm/deg.C over the operating temperature range of -40 to +85 deg. C.

The delay line is provided in a 24-pin DIP package, fully encapsulated in epoxy resin and is housed in a Diallyl Phthalate case, green in color. The case marking is applied by silkscreen using white epoxy paint. The 9 copper leads are tin-lead plated and meet the solderability requirements of MIL-STD-202, Method 208.

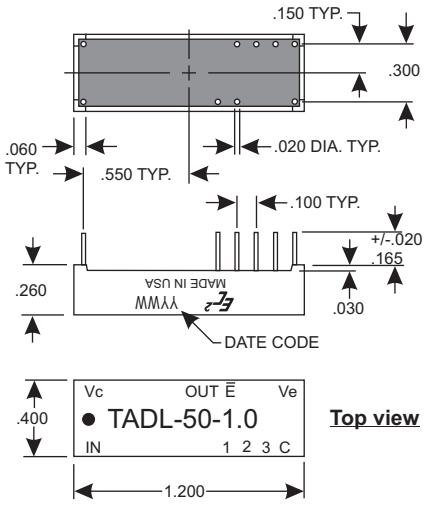
Operating Specifications:

All measurements made at 25 deg. C
All measurements made with Vcc = +5VDC
All measurements made with Vee = -5VDC
All measurements made with a sine wave:
  For step zero = 100 ns or less, 10MHz
  For step zero greater than 100ns, 7 MHz
All measurements made with a 100K ohms output load
Delays measured at 50% level on the leading edge

Input Impedance is 100 ohms +/-10%
Output Impedance is 170 ohms typical
Supply current < 1mA typical
Multiplexer setup time is 24 ns typical
Operating Temperature: -40 to +85 deg. C
Storage Temperature: -55 to +125 deg. C
Analog Input voltages should not exceed the Vcc supply
Analog Input voltages should not exceed the Vee supply

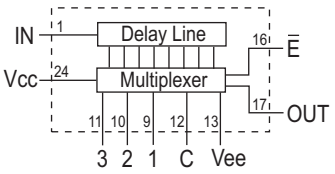
Programming and Enable pins:
  "Low" level input voltage: 2.0V min.
  "High" level input voltage: 0.8V max.
  Input Leakage current: 1uA max.

MECHANICAL DIAGRAM



Top view

BLOCK DIAGRAM



TRUTH TABLE

Example: TADL-50-1.0

Prog. Pins			Output
3	2	1	Delay
0	0	0	*50.0
0	0	1	**1.0
0	1	0	**2.0
0	1	1	**3.0
1	0	0	**4.0
1	0	1	**5.0
1	1	0	**6.0
1	1	1	**7.0

Product Selection Table

Part Number	*Step Zero Delay Time (nS)	Nominal Maximum Delay Time (nS)	Delay Change Per Step	**Maximum Deviation From Programmed Delay	-3dB Bandwidth (in MHz)
TADL-5.0-0.5	5.0+/-0.5	8.5	0.5+/-0.4	+/-0.5	50
TADL-10.0-0.5	10.0+/-0.7	13.5	0.5+/-0.4	+/-0.5	44
TADL-15.0-0.5	15.0+/-0.9	18.5	0.5+/-0.4	+/-0.5	38
TADL-20.0-0.5	20.0+/-1.1	23.5	0.5+/-0.4	+/-0.5	34
TADL-25.0-0.5	25.0+/-1.3	28.5	0.5+/-0.4	+/-0.5	30
TADL-30-1.0	30.0+/-1.5	37.0	1.0+/-0.7	+/-1.0	26
TADL-40-1.0	40.0+/-2.0	47.0	1.0+/-0.7	+/-1.0	23
TADL-50-1.0	50.0+/-2.5	57.0	1.0+/-0.7	+/-1.0	21
TADL-60-1.0	60.0+/-2.5	67.0	1.0+/-0.7	+/-1.0	19
TADL-80-1.0	80.0+/-3.0	87.0	1.0+/-0.7	+/-1.0	17
TADL-100-1.5	100.0+/-4.0	110.5	1.5+/-1.0	+/-1.5	14
TADL-150-1.5	150.0+/-5.5	160.5	1.5+/-1.0	+/-1.5	12
TADL-200-1.5	200.0+/-7.5	210.5	1.5+/-1.0	+/-1.5	9
TADL-250-1.5	250.0+/-10.0	260.5	1.5+/-1.0	+/-1.5	7

*Step zero is referenced to the input pin.
**Delay times after step zero are referenced to step zero.
Special modules can often be manufactured to provide for customer specific applications.

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