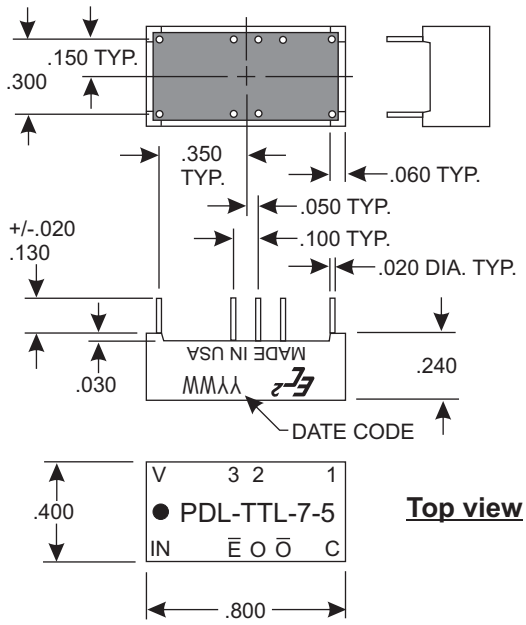
3-Bit Programmable TTL Logic Delay Line

The 3-Bit Programmable TTL Logic Delay Lines manufactured by Engineered Components Company are designed to provide output waveforms that reproduce the input waveform after a set amount of delay time has elapsed. The final delay of the output waveform can be adjusted during or after installation into a circuit. The adjustment is made by applying a logic "0" or "1" at each of the 3 multiplexor programming pins (see the Truth Table Examples). These delay lines are calibrated at the non-inverted output, but an inverted output and an enable pin are provided as well. The Enable pin is active low, and when high, the output is for forced low. The delay times are calibrated to the listed tolerances on the rising edge delays (see the Product Selection Table).

The MTBF on these modules, when calculated per MIL-HDBK-217, for a 50 deg.C ground fixed environment and with 50VDC applied, is in excess of 1.5 million hours. The temperature coefficient of delay is less than 500 ppm/deg.C over the operating temperature range of 0 to +70 deg. C.

The module is provided in a 16-pin DIP package, fully encapsulated in epoxy resin and is housed in a Diallyl Phthalate case, blue in color. The case marking is applied by silkscreen using white epoxy paint. The 9 copper leads are tin-lead plated and meet the solderability requirements of MIL-STD-202, Method 208.

MECHANICAL DIAGRAM



Product Selection Table

Part Number	Output Delays and Tolerances (in ns) *Step Zero Delay	Step-toStep Delay	Maximum Delay (Nominal)	** Maximum Deviation From Programmed Delay
PDL-TTL-7-1	7.0+/-1.0	1.0+/-0.3	14.0	+/-0.4
PDL-TTL-7-2	7.0+/-1.0	2.0+/-0.4	21.0	+/-0.6
PDL-TTL-7-3	7.0+/-1.0	3.0+/-0.5	28.0	+/-0.8
PDL-TTL-7-4	7.0+/-1.0	4.0+/-0.5	35.0	+/-0.9
PDL-TTL-7-5	7.0+/-1.0	5.0+/-0.5	42.0	+/-1.0
PDL-TTL-7-6	7.0+/-1.0	6.0+/-0.6	49.0	+/-1.2
PDL-TTL-7-7	7.0+/-1.0	7.0+/-0.7	56.0	+/-1.4
PDL-TTL-7-8	7.0+/-1.0	8.0+/-0.8	63.0	+/-1.6
PDL-TTL-7-9	7.0+/-1.0	9.0+/-0.9	70.0	+/-1.8
PDL-TTL-7-10	7.0+/-1.0	10.0+/-1.0	77.0	+/-2.0
PDL-TTL-7-11	7.0+/-1.0	11.0+/-1.1	84.0	+/-2.2
PDL-TTL-7-12	7.0+/-1.0	12.0+/-1.2	91.0	+/-2.4
PDL-TTL-7-13	7.0+/-1.0	13.0+/-1.3	98.0	+/-2.6
PDL-TTL-7-14	7.0+/-1.0	14.0+/-1.4	105	+/-2.8
PDL-TTL-7-15	7.0+/-1.0	15.0+/-1.5	112	+/-3.0
PDL-TTL-7-20	7.0+/-1.0	20.0+/-2.0	147	+/-4.0
PDL-TTL-7-25	7.0+/-1.0	25.0+/-2.5	182	+/-5.0
PDL-TTL-7-30	7.0+/-1.0	30.0+/-3.0	217	+/-6.0
PDL-TTL-7-35	7.0+/-1.0	35.0+/-3.5	252	+/-7.0
PDL-TTL-7-40	7.0+/-1.0	40.0+/-4.0	287	+/-8.0
PDL-TTL-7-45	7.0+/-1.0	45.0+/-4.5	322	+/-9.0
PDL-TTL-7-50	7.0+/-1.0	50.0+/-5.0	357	+/-10.0

* Delay at step zero is referenced to the input pin.

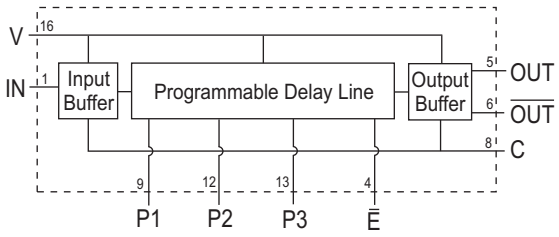
**All delay times after step zero are referenced to step zero.

TRUTH TABLE EXAMPLES (Delay times in ns)

Part Number									
	Programming Pin 3	0	0	0	0	1	1	1	1
	Programming Pin 2	0	0	1	1	0	0	1	1
	Programming Pin 1	0	1	0	1	0	1	0	1
PDL-TTL-7-1		7	1	2	3	4	5	6	7
PDL-TTL-7-5		7	5	10	15	20	25	30	35

Special modules can often be manufactured to provide for customer specific applications.

BLOCK DIAGRAM



Operating Specifications:

All measurements made at 25 deg. C
All measurements made with Vcc = +5VDC
All measurements made with (1) TTL output load

Operating Temperature: 0 to +70 deg. C
Storage Temperature: -55 to +125 deg. C

Vcc Supply Voltage: 4.75 to 5.25VDC
Vcc Supply Current = 90mA typical
Logic "High" Input:
Voltage: 2.0VDC min. ; Vcc max.
Current: 2.7VDC = 50uA max. ; 5.5VDC = 1mA max.
Logic "Low" Input:
Voltage: 0.8 VDC max.
Current: -2.0mA max.
Logic "High" Voltage Out: 2.7VDC min.
Logic "Low" Voltage Out: 0.5VDC max.
Multiplexor setup time = 4ns typ.

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