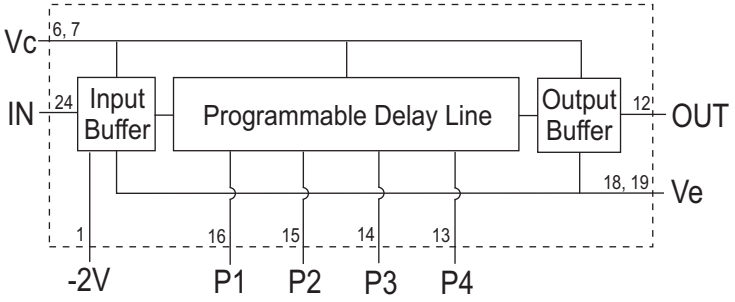
4-Bit Programmable 100K ECL Logic Delay Line

The 4-Bit Programmable 100K ECL Logic Delay Lines manufactured by Engineered Components Company are designed to provide output waveforms that reproduce the input waveform after a set amount of delay time has elapsed. The final delay of the output waveform can be adjusted during or after installation into a circuit. The adjustment is made by applying a logic "0" or "1" at each of the 4 multiplexor programming pins (see the Truth Table Examples). The delay times are calibrated to the listed tolerances on the rising edge delays (see the Product Selection Table). Negative 2.0VDC must be applied to the "-2V" lead (pin1)

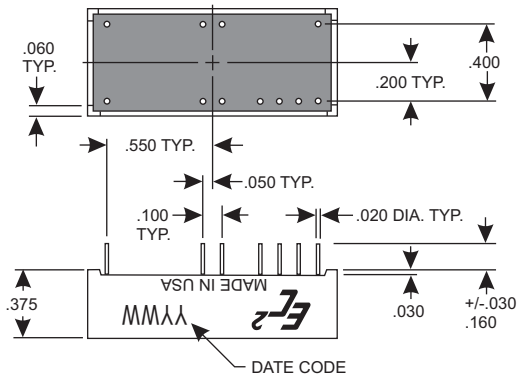
The MTBF on these modules, when calculated per MIL-HDBK-217, for a 50 deg.C ground fixed environment and with 50VDC applied, is in excess of 0.75 million hours. The temperature coefficient of delay is less than 150 ppm/deg.C over the operating temperature range of 0 to +85 deg. C.

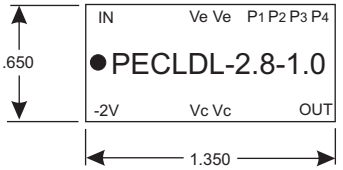
The module is provided in a 24-pin DIP package, fully encapsulated in epoxy resin and is housed in a Diallyl Phthalate case, blue in color. The case marking is applied by silkscreen using white epoxy paint. The 11 copper leads are tin-lead plated and meet the solderability requirements of MIL-STD-202, Method 208.

BLOCK DIAGRAM



MECHANICAL DIAGRAM





Top view

Product Selection Table

Part Number	Output Delays and Tolerances (in ns) *Step Zero Delay	Step-toStep Delay	Maximum Delay (Nominal)	** Maximum Deviation From Programmed Delay
PECLDL-2.8-0.1	3.8+/-0.6	0.1+/-.04	4.3	+/-0.10
PECLDL-2.8-0.2	2.8+/-0.6	0.2+/-.05	5.8	+/-0.20
PECLDL-2.8-0.3	2.8+/-0.6	0.3+/-.10	7.3	+/-0.25
PECLDL-2.8-0.4	2.8+/-0.6	0.4+/-.10	8.8	+/-0.30
PECLDL-2.8-0.5	2.8+/-0.6	0.5+/-.15	10.3	+/-0.35
PECLDL-2.8-0.6	2.8+/-0.6	0.6+/-.15	11.8	+/-0.40
PECLDL-2.8-0.7	2.8+/-0.6	0.7+/-.20	13.3	+/-0.45
PECLDL-2.8-0.8	2.8+/-0.6	0.8+/-.20	14.8	+/-0.50
PECLDL-2.8-0.9	2.8+/-0.6	0.9+/-.20	16.3	+/-0.50
PECLDL-2.8-1.0	2.8+/-0.6	1.0+/-.20	17.8	+/-0.50
PECLDL-2.8-1.5	2.8+/-0.6	1.5+/-.25	25.3	+/-0.80
PECLDL-2.8-2.0	2.8+/-0.6	2.0+/-.25	32.8	+/-1.00
PECLDL-2.8-2.5	2.8+/-0.6	2.5+/-.30	40.3	+/-1.30
PECLDL-2.8-3.0	2.8+/-0.6	3.0+/-.30	47.8	+/-1.50
PECLDL-2.8-3.5	2.8+/-0.6	3.5+/-.35	55.3	+/-1.80
PECLDL-2.8-4.0	2.8+/-0.6	4.0+/-.40	62.8	+/-2.00
PECLDL-2.8-4.5	2.8+/-0.6	4.5+/-.45	70.3	+/-2.30
PECLDL-2.8-5.0	2.8+/-0.6	5.0+/-.50	77.8	+/-2.50

* Delay at step zero is referenced to the input pin.

**All delay times after step zero are referenced to step zero.

TRUTH TABLE EXAMPLES (Delay times in ns)

Part Number	Programming Pin 4	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	Programming Pin 3	0	0	0	0	1	1	1	0	0	0	0	1	1	1	1
	Programming Pin 2	0	0	1	1	0	0	1	0	0	1	1	0	0	1	1
	Programming Pin 1	0	1	0	1	0	1	0	0	1	0	1	0	1	0	1
PECLDL-2.8-1		2.8	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
PECLDL-2.8-5		2.8	5	10	15	20	25	30	35	40	45	50	55	60	65	70	75

Special modules can often be manufactured to provide for customer specific applications.

Operating Specifications:

All measurements made at 25 deg. C
All measurements made with Ve = -4.5VDC, Vc = 0VDC
All measurements made with (1) 100K ECL output load
All measurements made with a 50 ohm pulldown resistor to -2VDC at the input and output

Operating Temperature: 0 to +85 deg. C
Storage Temperature: -55 to +125 deg. C

Vee Supply Voltage: -4.5 +/-5% VDC
Vcc Supply Current: 140mA typical
Logic "High" Input:
Voltage: -1.165VDC min.
Current: 350uA max.
Logic "Low" Input:
Voltage: -1.475VDC max.
Current: 0.5uA min.
Logic "High" Voltage Out: -1.025VDC min.
Logic "Low" Voltage Out: -1.625VDC max.
Multiplexor setup time = 1ns typ.

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