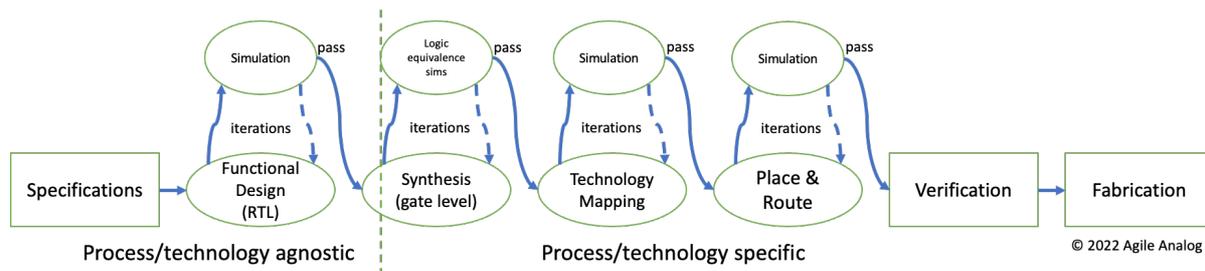


Title: Agile Analog’s Approach to Analog IP Design and Quality --- Why “Silicon Proven” is NOT What You Think

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The complexity of integrated circuit design has expanded a billion-fold since the invention of the first transistor, guided by the famous “Moore’s Law” of semiconductor manufacturing. An important factor to this ever-growing expansion is the development of the digital design flow. A modern digital design consists of several steps, a simplified flow chart is shown below:



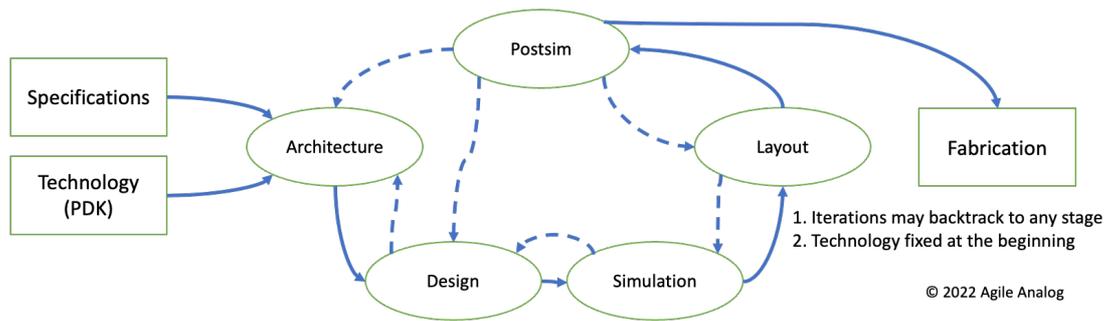
Digital design is initially done in a largely process agnostic way, guided mostly by the likely logic depth and its impact on the achievable performance. This enables excellent design portability between process nodes, without impacting verification quality. A comprehensive design tool flow and verification methodology to check consistency and compliance at each stage of the flow has enabled a huge growth in designer productivity as the level of design capture abstraction has increased. Along with the improved verification and signoff tools, it has enabled the automation of the digital design process to generate complex, high quality, right-first-time IC’s that no longer rely on silicon validation for proof.

Although the digital design is process independent, the implementation of the design from synthesis through place and route takes full consideration of the target process node through the various models and signoff processes. Indeed, the same design can be implemented in a very different way and optimized to take advantage of the specific process features.

The process agnostic digital design allows full IP reuse across projects and product generations within a company. This is a key reason why the digital IP business model has continuously grown and thrived over the years. The digital implementation process flow is process-specific and allows companies to reuse digital designs while keeping up with the newest generation of semiconductor manufacturing technology.

Over the past three decades digital design flow has been proven, improved and optimized, such that a first-cut design success is expected, even in the most advanced technology nodes.

On the other hand, the analog design flow is very different:



While there are analogies between the analog design flow and digital design flow, for example the “architecture” in analog flow is akin to the “functional design” in digital flow, and “layout” in analog flow to “place and route” in digital flow, there are distinguishing differences between the two.

First, the analog design flow is a circular iteration of several cycles, different from the “linear” digital design flow. Depending on the complexity of the analog circuit block, experience of the circuit designer, expertise in the technology node, and many other factors, the design flow will iterate several times in the analog design flow loop, often between layout and postsim steps. In some cases, the architecture chosen cannot fulfill the circuit specifications in the physical level, resulting in a restart from the first step. Simply speaking, the time and effort needed to complete an analog circuit are approximations, and the uncertainty increases as the complexity increases or change in technology.

Second, the technology or process node of an analog IP is decided at the beginning of the design, the available devices for architecture exploration and design, model cards for simulation, layout rules, and the metal R-C models are all process specific. If a project manager decided to change the process node, or even modify the process options available for use, the whole analog design often must start from square one.

Finally, there is very little CAD automation in each step of the analog design process. While there are excellent EDA tools for each design step, the different analog blocks have different design methods, simulations are circuit, process, and application dependent, and layout is fully custom.

The below table summarizes the key differences between analog and digital design methods, and these differences are the reasons why analog design takes more time, not easily scalable, and exclusive compared to digital designs.

	Design Flow	Process	CAD automation
Digital Design Flow	Linear	Fairly independent	High
Analog Design Flow	Circular	Highly dependent	Low

What makes a good analog IP? More specifically, what is needed to create a good analog IP?

First, we need to choose a good circuit architecture that is stable, robust, and suitable for mass production.

Up-to-date PDKs (Process Development Kit) from foundries provide front-end (transistors, varactors, diodes, etc.) and back-end (resistors, capacitors, metals, etc.) models for simulation, various command files for DRC, LVS, and parasitic extraction. PDKs nowadays from major foundries have very good correlation between model and physical silicon. A proper PDK installation and choosing the process option is all that needs to be done.

Thorough behavior simulation and detailed circuit simulations at the required PVT (process, voltage, and temperature) corners will assure that the circuit will operate as expected. Circuit layout requires knowledge of the circuit of design, knowledge of process effects to analog performance, and meticulous attention to the details of every single trace.

The work above requires a seasoned team of experienced circuit designers and layout engineers with multiple-domain knowledge. For example, an analog circuit designer needs to have a working knowledge of layout rules and placement guidelines as well as the main process effects to the circuit performance, and a layout engineer need be able to identify the key requirements for each trace, whether a trace is for power, general signal, or sensitive signal.

With a good circuit architecture, accurate PDK, thorough simulations, detailed layout, and an experienced team to execute through the analog design flow, a high-quality analog IP will be delivered with minimum rounds of iterations through the design flow.

Good analog design teams are scarce and hard to come by, and high-quality analog IPs are rare and are quite valuable in the market as well. This often leads to the question from IC design companies whether a particular analog IP is “silicon proven” or requiring an analog IP to be “silicon proven” to be qualified for use. Hence, we come to the fundamental questions are, “what is silicon proven?” and “is silicon-proven proof of IP quality?”

The general definition of a “silicon-proven” IP is an IP that has been manufactured on silicon and its functionality bench-test measured, hence verified “on-silicon”. Once an IP is “silicon-proven”, it gains credibility that it will work as expected on a production chip, with the identical layout on the same process technology. However, such a silicon proof is only a single-point (or several points) validation of the design, usually based on pre-defined parameters and measured at specific voltage and temperature points; in other words, a “sample” of the IPs capabilities. Whether this “silicon proven” IP is “production quality” is determined before the manufacturing of this IP: the architecture chosen, the comprehensive simulations and design corners covered, the diligence put in the layout, and the effort in verification during development. In other words, an IP that is “silicon-proven” is merely a sanity check, only proving that the IP development flow “seems” to be “okay.” This does not seem to be a sufficient proof of quality.

Some “silicon-proven” IPs are IPs extracted from production chips, or used by other licensees in successful production, which have endured real-world high-volume tests under all sorts of conditions. These IPs certainly have credibility in its quality. However, these IPs are designed specifically for a particular product in a particular process node; for a project in a different node, process-porting is required, thus nullifying its “silicon-proven” status. In the case where a new project is using the exact node as the silicon verified IP, the IP may not match your need in terms of performance or area. For example, the PMOS driving device consists of over 50% of the entire LDO area, a “silicon-proven” LDO is often over-designed for one’s need, costing more silicon area than necessary. The dimensions are also fixed, so the other components need to fit the dimensions of the IP. Modifications to these silicon-proven IPs are possible, but the additional cost in money (\$xxx k) and time (6 months to a year) for each instance is quite often too high to bear. Modifications also invalidates the “silicon-proven” status of the original IP.

Process choice, process option, design parameters over corners, functions are all factors determining the “silicon-proven” validity of the IP. Shown in table form, it is clear that “silicon-proven” is very rare in IP reuse.

	Re-use	Re-use	Re-use	Reuse	Re-use	Re-use
Process Choice	Identical	Identical	Identical	Identical	Identical	Different
Process Options (e.g. metal stack)	Identical	Different	Identical	Identical	Different	Different
Design/test parameters over corners	Identical	Identical	Different	Identical	Different	Identical
Function/features	Identical	Identical	Identical	Different	Different	Identical
Silicon Proven?	Yes	Possible	Possible	Less Likely	Unlikely	NO

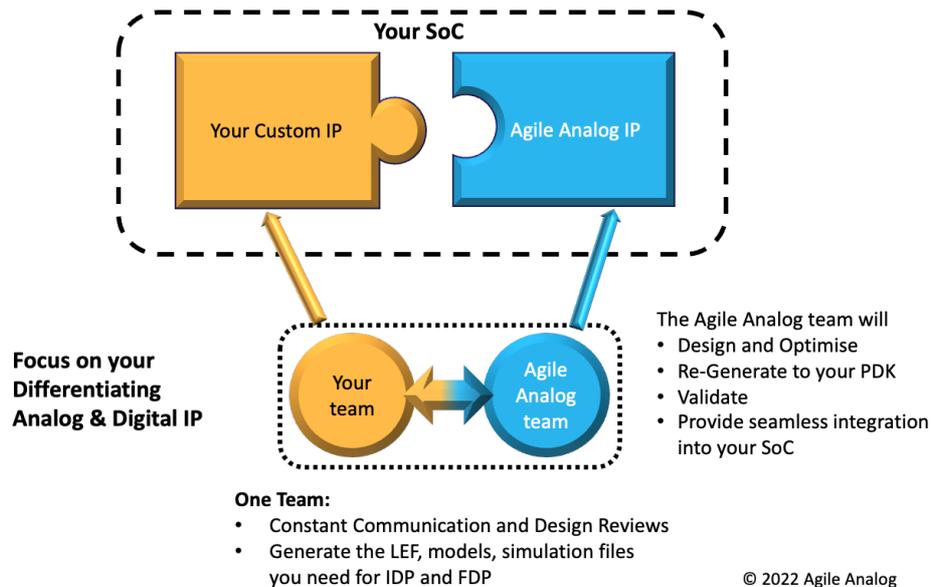
In summary, “silicon-proven” IPs are tied to certain processes with defined performances and validated at specific points of the design parameters. They may not match one’s need, and modifications to the IPs most likely invalidate their “silicon-proven” statuses. The quality of an analog IP is still based on the criteria addressed in the previous section, namely: good architecture, accurate PDK, thorough simulations, experienced design team, and a rigorous design flow to connect all these qualities together.

At Agile Analog, we have an experienced analog design team, with decades of experience with all sorts of analog and mixed-mode IPs. Our designers have designed and delivered analog IPs across standard CMOS processes, in both mature and advanced nodes, as well as specialty CMOS processes such as SOI and BCD processes.

In addition, Agile Analog’s core technology is a “formal-flow” to the so-called “art” of analog circuit design. By applying software automation via rules-based AI to the generation of the IP and to the design flow, we are developing and delivering analog IPs in a revolutionary way. Our method not only defines the schematic, the “what” of the IP, but also the intent and the essence of the design, which is the “why” and the “how” an IP works. This allows us to develop and generate an IP in any process node, and the automated, comprehensive verification flow assures the performance and quality of the IP for every delivery.

Taking advantage of Agile Analog’s IP generation engine, we can deliver analog IPs tailored to the specific needs of each customer. The specifications are “exactly to spec,” optimized for area and performance. For the “front-end” portion of the project, Agile Analog’s initial deliverables include behavior models for system simulations. The behavior models are process-independent, which means that analog IPs can be introduced early in the system design flow, allowing customers to plan and simulate the system including the analog IPs early in product development. For the “back-end” portion of the project, in the case of a PDK update from the foundry, regeneration or re-verification of the IP can be quickly done. It is also possible to evaluate IP performance across different process nodes or device options.

Fundamental analog IPs such as power management (PMU), sensors, and data processing (ADC & DAC) are essential blocks in every SoC, but due to its repetitiveness, maturity in design and domain knowledge, these tasks are often mundane and unexciting to an analog expert. Agile Analog’s ability to repeatedly generate these fundamental IPs allows customers to focus their team and experts on their differentiating analog and mixed mode designs, i.e., the “added-value” portion or “secret sauce” of their product.



A customer's product lineup usually consists of several chips of varying features and configurations, which Agile Analog can sufficiently support by generating an assortment of analog IPs to meet each chip's specific requirements. In addition, Agile Analog can also generate IPs in any process node of customer's choice, as a customer migrates to newer process nodes, Agile Analog's IP delivery can follow customer's development roadmap. Our automation technology brings consistency to our IP generation and delivery across technologies. Automation also applies to our quality checks, meaning less sensitive to human interference, and continuous improvement as new rules and features are added to our flow. Gone are the days of finding new analog IP vendors every time one migrates to a new technology node, Agile Analog can do it all.

Good architecture, thorough design and simulation, quality layout, and following a formal and automated design flow that ensure the above criteria are met at every step are the essential elements to developing high-quality analog IPs. Agile Analog's experienced design team and our IP generation engine assures that our deliverables will meet the quality and performance that our customers and the IC industry demands. Through our formal flow and automation, Agile Analog can deliver high quality analog IPs for all process nodes and optimized to customer's individual needs in a repeatable and timely manner.

Agile Analog's customer can kick-off a project with the assurance that the fundamental analog IPs are available and will meet the project's specifications, without the need to shop around. Our approach to analog IP development can grow and evolve along with the customer, either horizontally across the product line, or vertically to newer technologies and process nodes.

Following the footsteps of the leaders in IC industry, Agile Analog is committed to bring success to our customers.

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About the author:

Michael Lei is an FAE for APAC region at Agile Analog. Michael began his career in 2007 as an RF circuit designer and has designed RF circuits, led RF projects, led SoC projects, launched new products, managed customer projects, and done technical marketing for new projects at several IC design companies in Taiwan and China. His expertise is in RF and analog circuits and systems for cellular, Wi-Fi, Bluetooth, and its use in IoT applications.

About Agile Analog:

Analog IP needs to be different for each design. That is why Agile Analog has made a new way of doing things, conceived by some of the best minds in the industry. We provide a wide range of analog IP that is customised to your needs quickly, to a higher quality, and on any semiconductor process. Contact us at www.agileanalog.com to find out more.