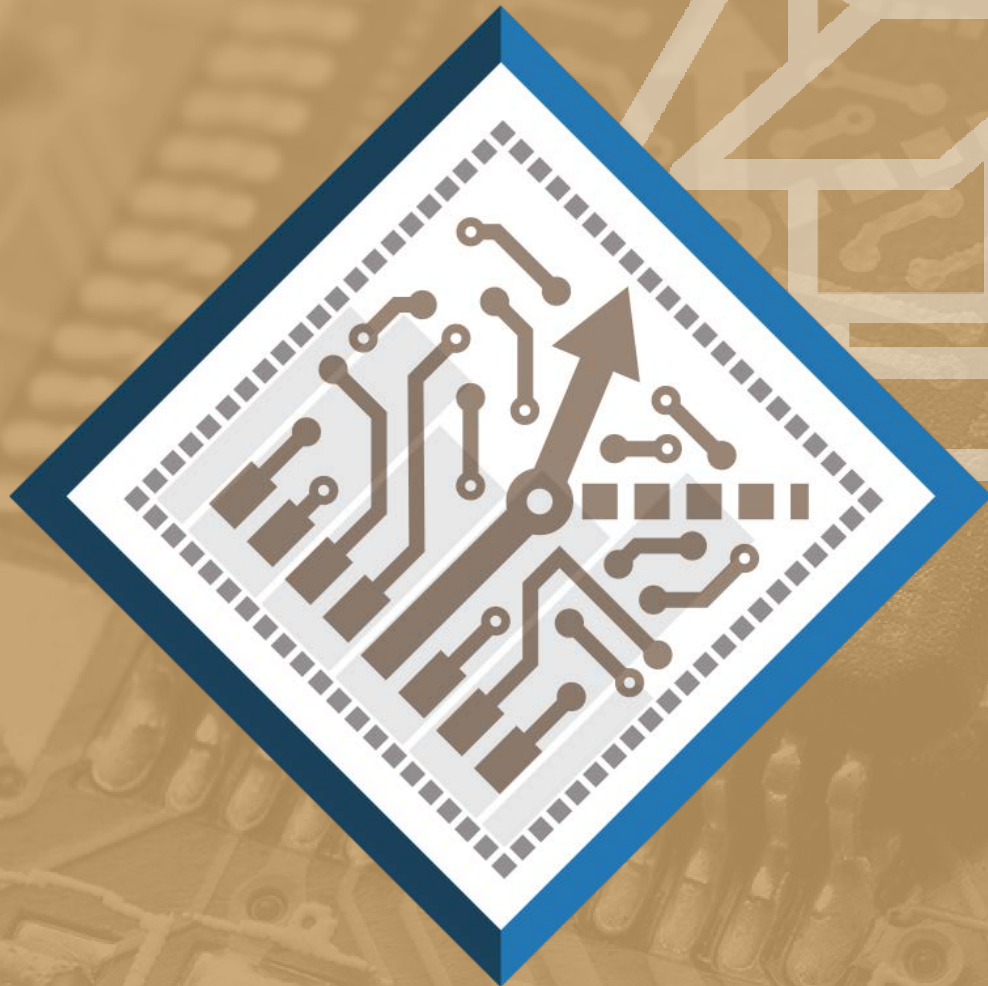
LINTON SALMON

PROGRAM MANAGER
DARPA/ MTO



3D MONOLITHIC SYSTEM ON A CHIP (3DSOC)

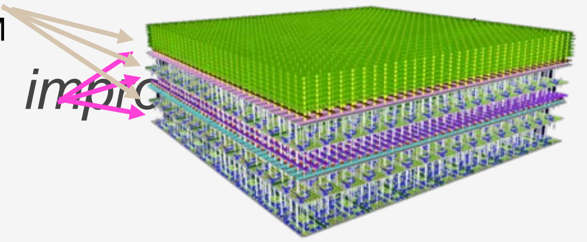
3DSOC PROGRAM

GOALS AND METRICS

Program Goal

Develop novel monolithic 3D fabrication technologies enable new architectures to drive a >50X SoC performance at power

12 layers of ReRAM interspersed with 5 layers of CNFET logic



Program Metrics

- 3DSoC technology capability of >50X Vs. 2D 7nm Performance at Power (PaP)
  - Interconnect densities > 9M interconnects/mm^2 between 3D layers
  - Interconnect bandwidth > 45Tb/s between 3D layers
  - On-die memory access energy < 2pJ/bit
- Yield > 30% for full 3DSoC designs
- Successful use of EDA flow for a > 500M gate/4GB memory 3DSoC design
- Capability to be fabricated as an on-demand foundry service for multiple DoD and commercial customers using a U.S. fabrication facility

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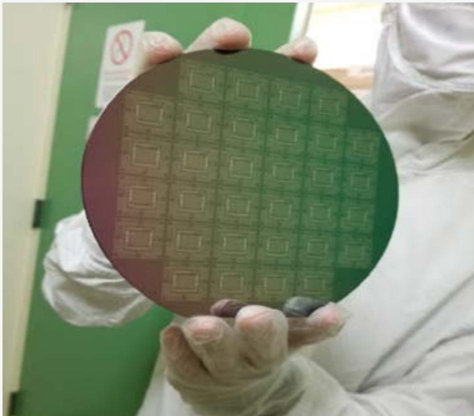
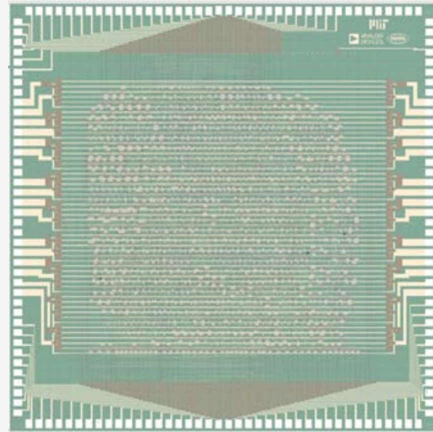
3DSOC PROGRAM

MAJOR ACCOMPLISHMENTS

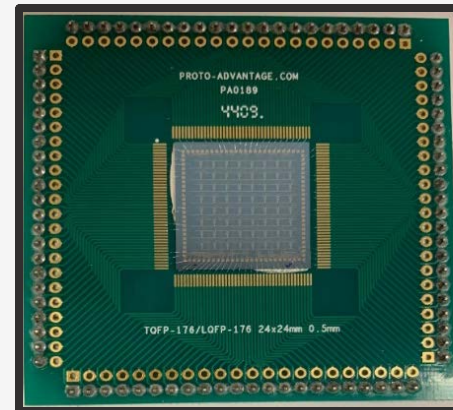
SkyWater 3DSoC Test Wafer



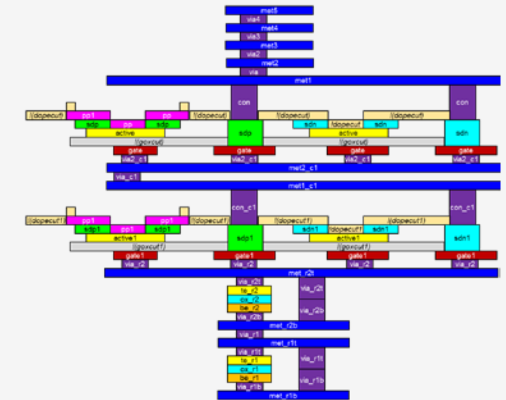
MIT CNFET ASIC



MIT Multi-Level CNFET Sensor



Calibrated Process Design Kit (PDK)



- Carbon Nanotube FETs (CNFETS) and Resistance Memory (RRAM) fabricated at SkyWater Technology Foundry
- Key CNFET building blocks demonstrated at MIT
  - Complex digital ASIC fabricated with CNFETs
  - Multi-level CNFET demonstrated
- Calibrated Process Design Kit (PDK) developed and delivered to alpha design teams

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3DSOC

PERFORMERS

MIT *PI: Max Shulaker (MIT)* *Co-PI: Mark Nelson (SkyWater)* *Co-PIs: Subhasish Mitra & Simon Wong (Stanford)*	 *CNFET development* *3DSoC Fabrication Foundry* *System Simulation & RRAM Development*
GA Tech *PI: Sung Kyu Lim (GA Tech)* *Co-PI: Saibal Mukhopadhyay (GA Tech)* *Co-PI: Krishnendu Chakrabarty (Duke)*	 *3DSoC Design Tool Development* *3DSoC Memory Design Development* *3DSoC Design for Testability*

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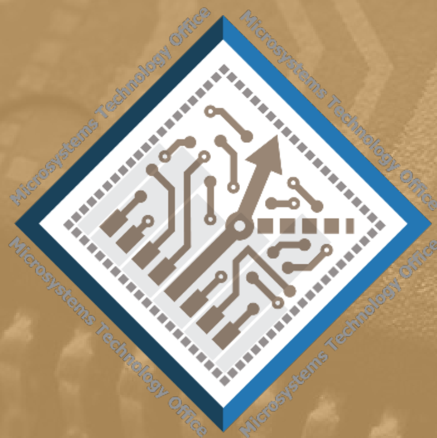

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