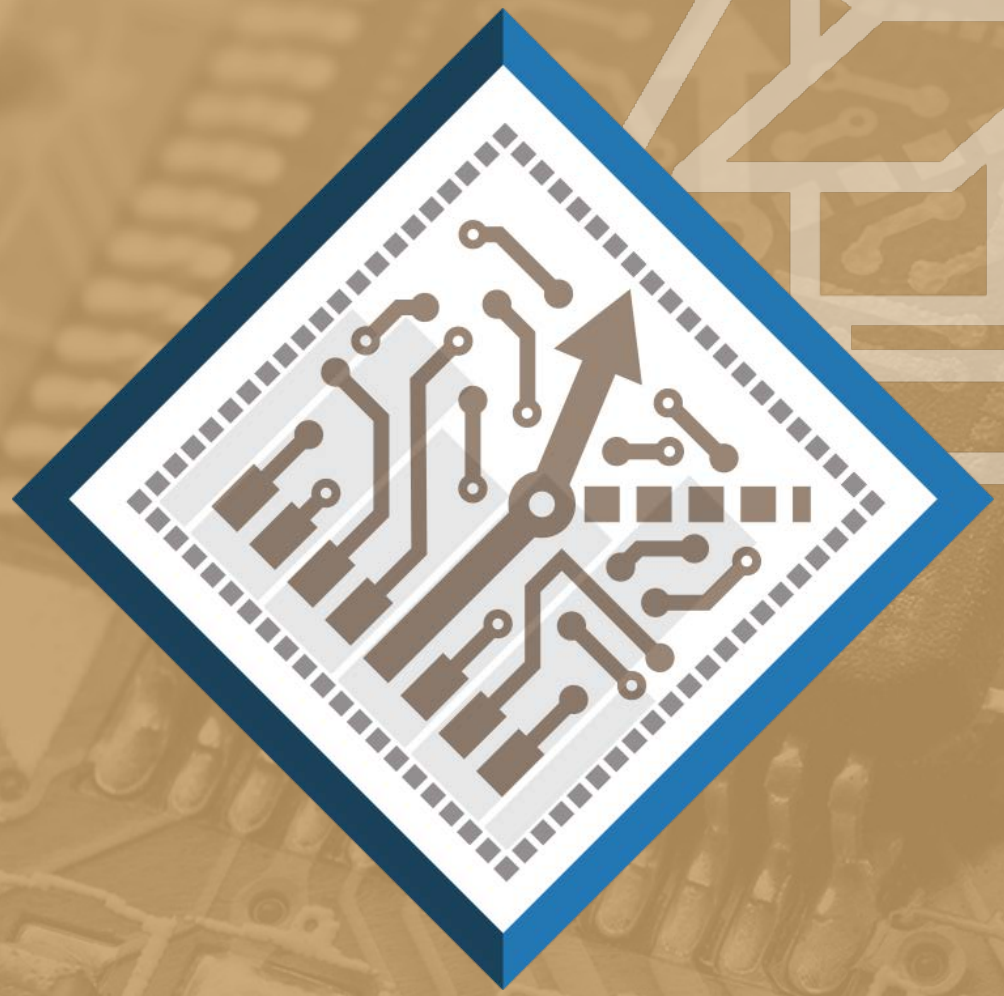
LINTON SALMON

PROGRAM MANAGER
DARPA/ MTO



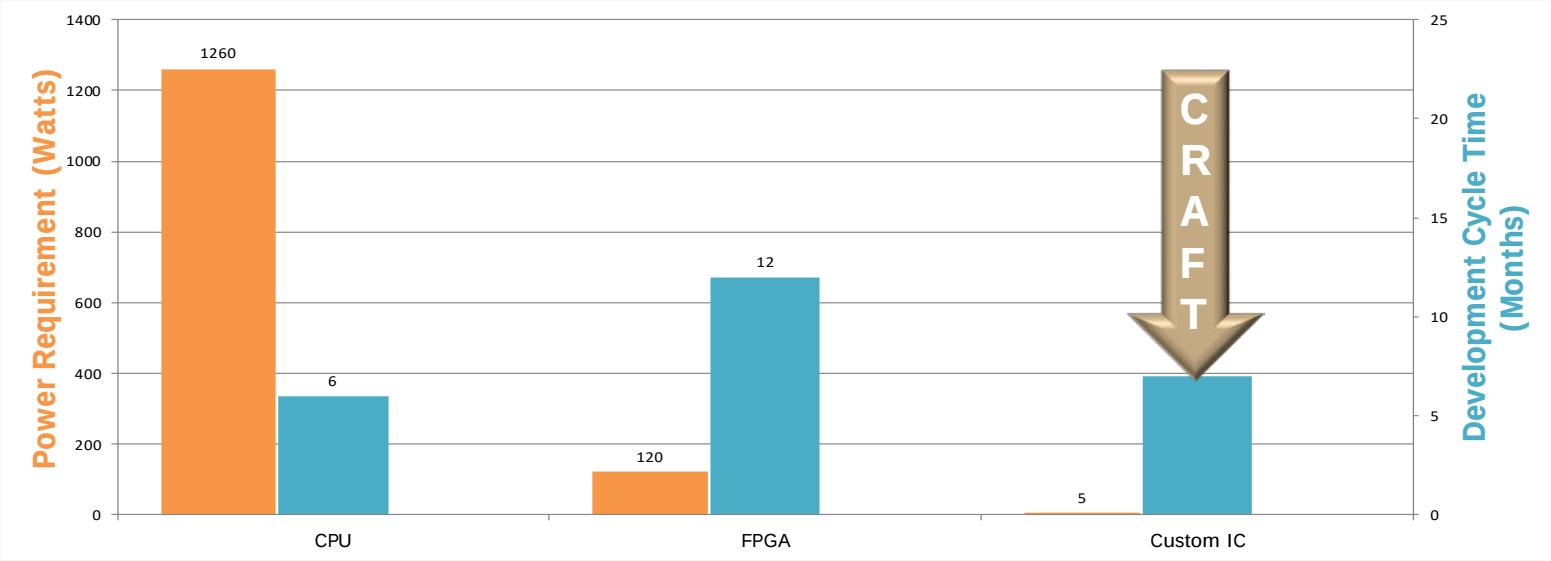
CIRCUIT REALIZATION AT FASTER TIMESCALES (CRAFT)

CRAFT PROGRAM

GOAL

Goal

- *To sharply reduce the barriers to DoD use of custom integrated circuits built using leading-edge CMOS technology while maintaining the high level of performance at power promised by this technology*



Example Data from representative DoD design

CRAFT

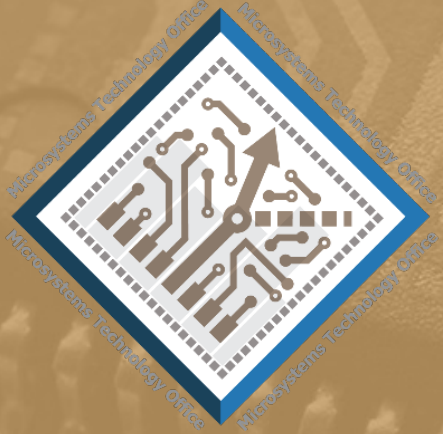
METRICS AND ACHIEVEMENTS

Metrics	Achievements
Reduce IC design cycle effort of custom ICs at leading edge nodes by 10X	11X-8X effort reduction achieved for both Analog and Digital designs on ICs taped out in Phase2 of CRAFT
Reduce design Port effort to new technologies by 5X	5.3X-4.3X effort reduction for porting to 16nm GF technology demonstrated on digital and mixed signal ASICs
Provide Access to 16nm technology through dedicated MPW runs	Three successful 16nm MPW runs made at TSMC and one in fabrication
Establish design repository and remote IC design environment to foster design reuse and utility by smaller design teams	Demonstrated CRAFT design flow, design repository and remote design environment for multiple teams to utilize the 16nm technology for Analog and Digital designs

CRAFT

PERFORMERS

University of California Berkeley *PI: Elad Alon*	*Utilize CHISEL and BAG for digital and analog design process optimization*
NVIDIA *PI: Brucek Khailany*	*High Level Synthesis for digital design process optimization*
USC-ISI *PI: Ewa Deelman*	*IP Repository and Remote IC Design environment (VAULT) setup*



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