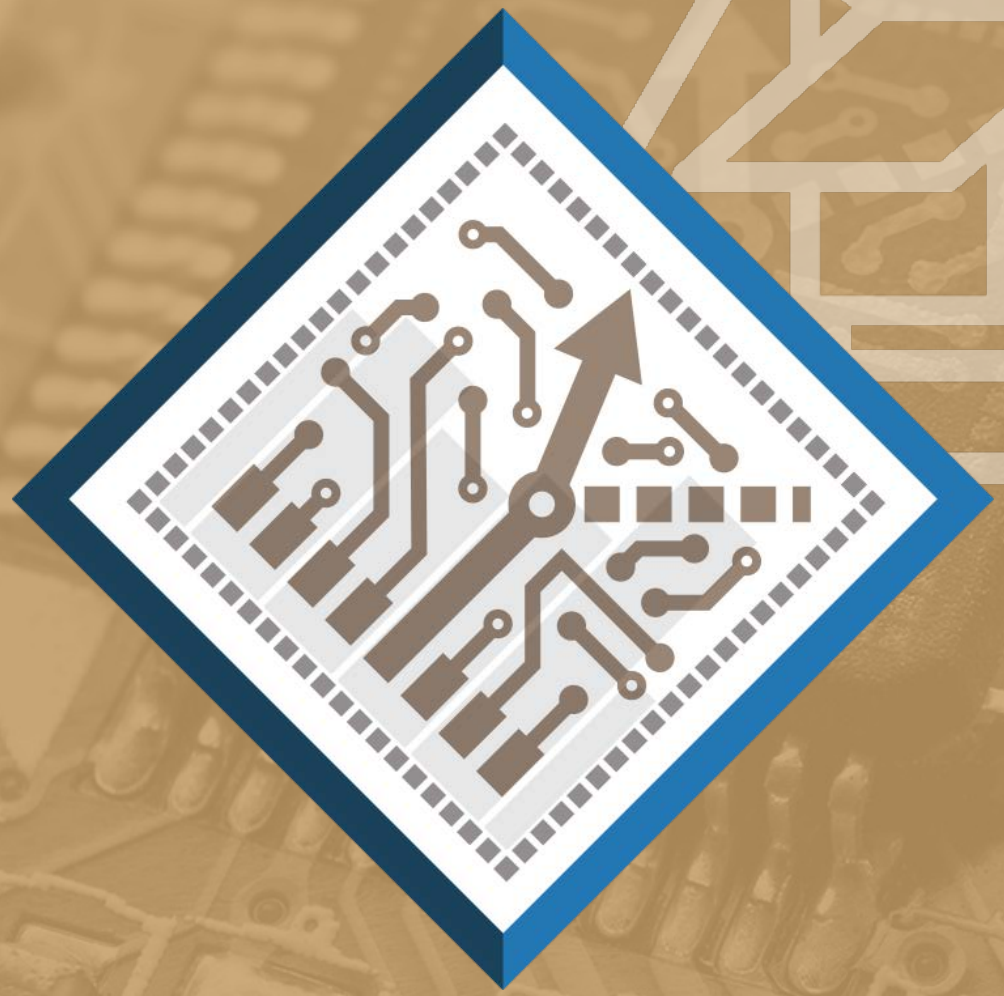
ANDREAS OLOFSSON

DARPA MTO
PROGRAM MANAGER



COMMON HETEROGENEOUS INTEGRATION AND IP REUSE STRATEGIES (CHIPS)

CHIPS

COMMON HETEROGENEOUS INTEGRATION AND IP REUSE STRATEGIES

DESIGN

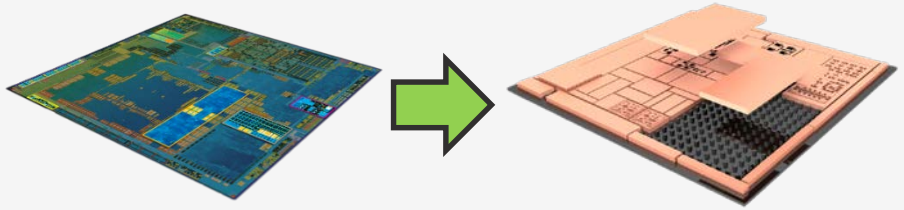
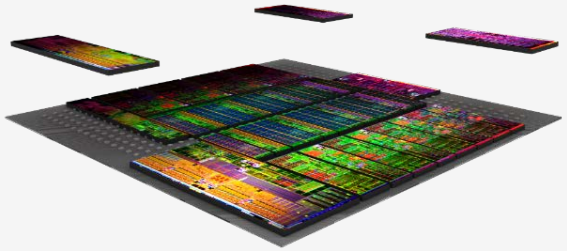


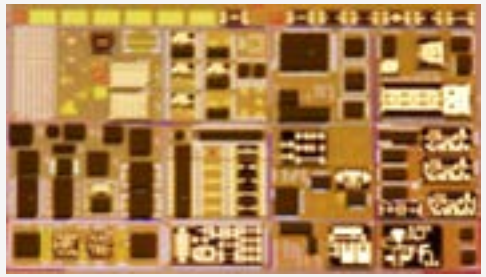
Image source: Intel

TECHNOLOGY

- ✓ A universal efficient interface standard
- ✓ SOTA manufacturing assembly
- ✓ A large and critical set of IP chiplets



Extend Moore's law
Scale out and scale down while managing yield

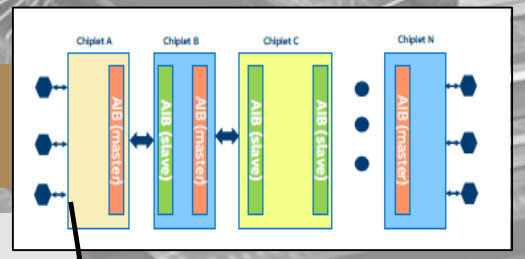


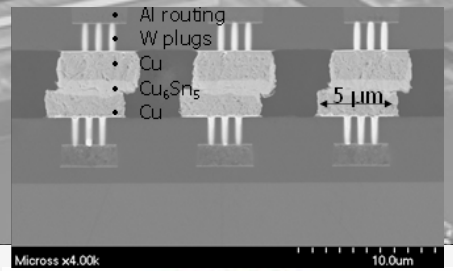
Enable heterogeneous integration
Materials/processes, companies, geography, security

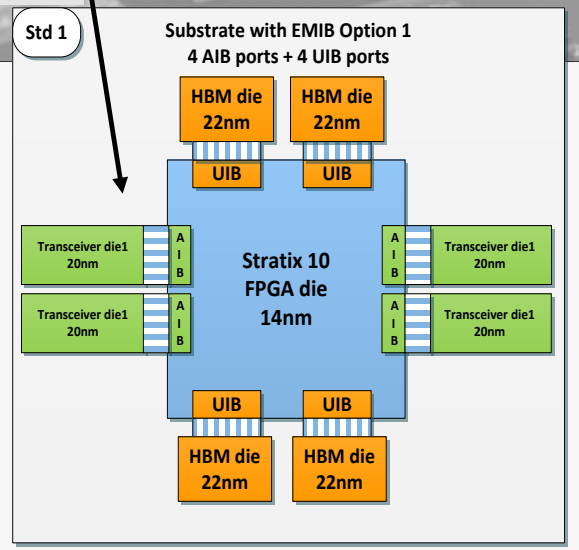
Empower system integrators
Democratize access to leading edge silicon for system integrators

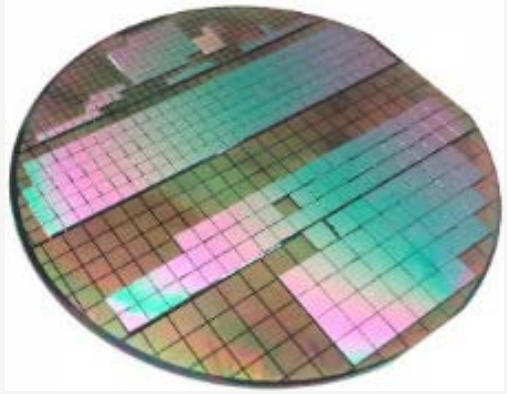
CHIPS

PHASE1 PROGRAM HIGHLIGHTS



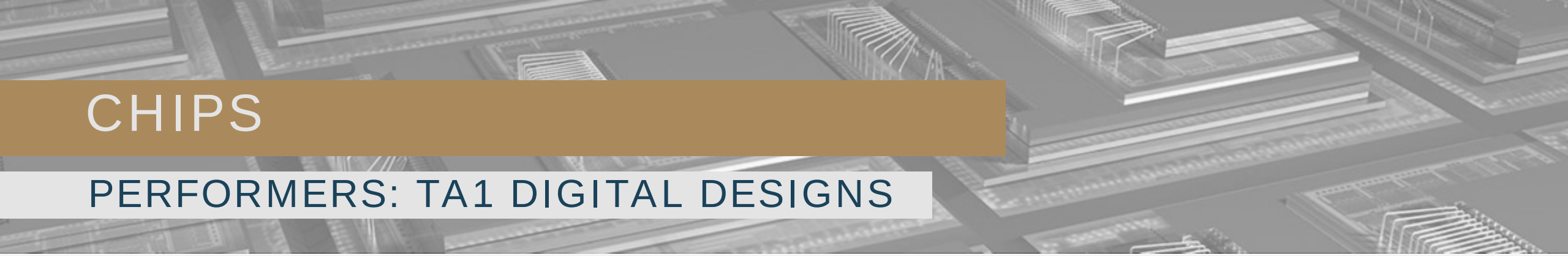






- Demonstrating world's highest throughput direct RF sampling RF/FPGA system
- Demonstrated record setting energy efficient chip-to-chip interface
- Demonstrated 10 µm pitch die-to-wafer copper interconnects
- First ever hardware standard released as an open source reference design

Metric	Target	Status
Interface Protocol	Common Standard	Met (AIB)
Energy Efficiency	1 pJ/bit	Met (AIB)
Latency	<5 ns	Met (AIB)
Bandwidth Density	1000 Gbps/mm	Q3 2019 Demo
IP Reuse	>50%	75% (Demo)



CHIPS

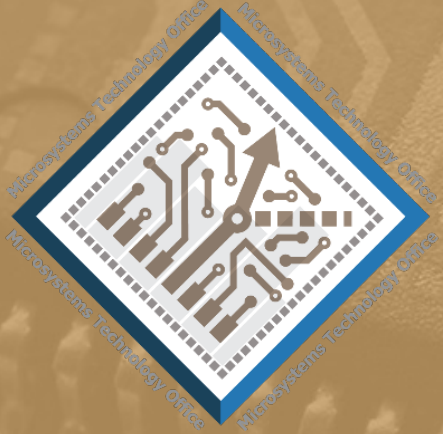
PERFORMERS: TA1 DIGITAL DESIGNS

Intel *PI: Sergey Shumarayev*	FPGA platform, AIB interface standard
University of Michigan PI: *Zhengya Zhang, Michael Flynn*	Deep learning chiplet integration
Lockheed Martin *PI: Kevin Thorson*	DoD obsolescence mitigation via modularity
Northrop Grumman Mission Systems *PI: Justin Parke*	ACT chip disaggregation, fine pitch integration

CHIPS

PERFORMERS: TA3 ASSEMBLY AND DESIGN

Georgia Tech (*PI: Sung-Kyu Lim)*	EDA tools, system analysis
Ferric (*PI: Noah Sturcken)*	System In Package PMIC
UCLA (P*I: Subu Iyer)*	10 μm pitch copper die-to-wafer interconnect fabric
Jariet Technologies: (*PI: Craig Hornbuckle)*	64 Gsps Quad ADC/DAC
Northrop Grumman / Synopsys (PI: *Jay Bacon)*	Leading edge memory controller chiplet
North Carolina State University (*PI: Paul Franzon)*	RISC-V and ML accelerator chipletization
Analog Devices (*PI: Rod Miller)*	10 Gsps ADC chiplet and KGD probing



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