Unprecedented Efficient Graph Analytics

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Qualcomm

Architectures Thrust: Hierarchical Identify Verify Exploit (HIVE)

Program Goals and Value Proposition

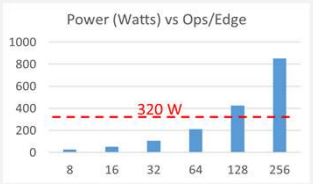
PERFORMANCE	10 GTEPs / Node	PROCESSING EFFICIENCY	100X in Hardware 10X in Software **1000X TOTAL**
ENERGY EFFICIENCY	0.5 GTEPs / W 2 nJ / TE		
MEMORY EFFICIENCY	90% both, random & sequential accesses		
DEMONSTRATION	16 nodes 160 GTEPs system	SCALABILITY	Beyond 16 nodes to Tera TEPs

Scalable 160 GTEPS system, consuming < 320 Watts

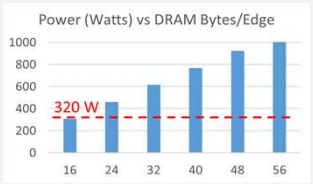
Enabling technologies for data analytics with unprecedented efficiency

Challenges: 160 GTEPS @ 320 W

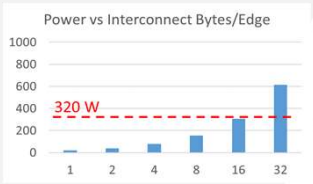
Compute



DRAM



Interconnect



Investigation priorities: (1) Intra-node data movement, (2) Interconnect, (3) Compute

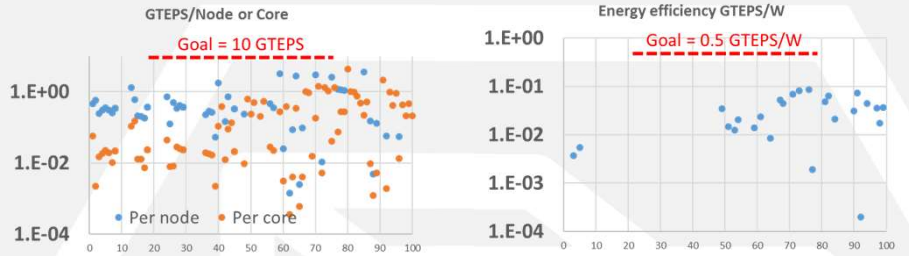
Memory Subsystem

- Intelligent memory controllers to improve data movement efficiency
- Fine-grain management
- Optimized data layout—HW/SW co-design with data analytics application

Interconnects

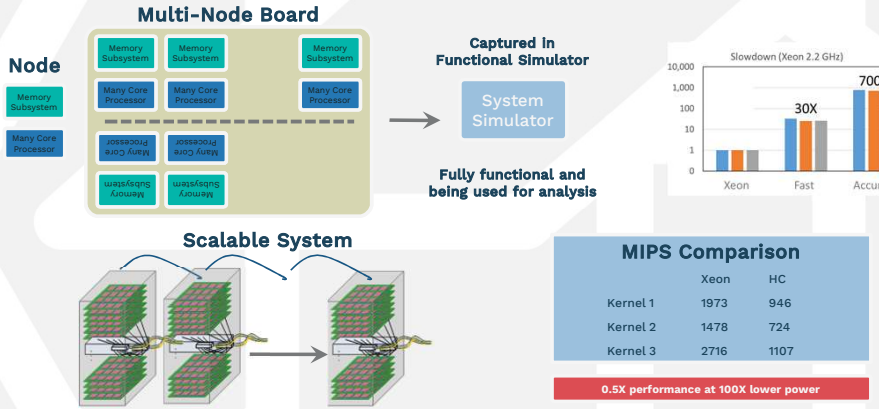
- Hierarchical & heterogeneous
- Hi Radix interconnect scheme with right balance
- Right balance of Electrical and Optical

HIVE Goals Compared to Graph-500 (Q4-2016)



Goals are even harder considering Graph-500 is probably not a good representative

System Architecture

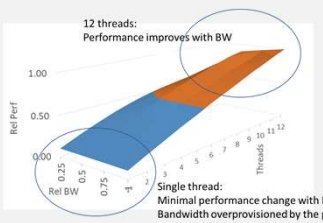


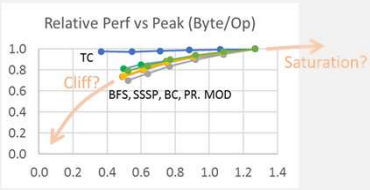
MIPS Comparison

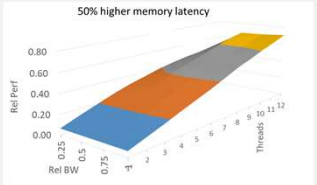
	Xeon	HC
Kernel 1	1973	946
Kernel 2	1478	724
Kernel 3	2716	1107

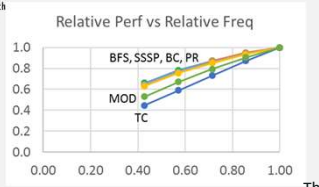
0.5X performance at 100X lower power

Workload Simulations & Analysis









Determine optimum Frequency, Memory BW, Latency, and Interconnect characteristics

Simulated Performance, Energy, Power

This research was developed with funding from the Defense Advanced Research Projects Agency (DARPA).
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