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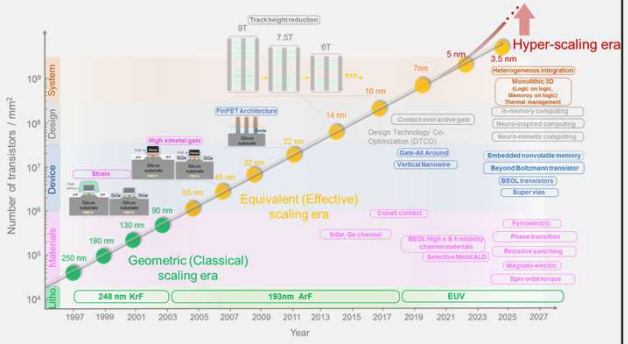
JUMP : Applications and Systems Driven Center for Energy-Efficient Integrated NanoTechnolgies (ASCENT)

Grand Challenge in Semiconductor Industry



Era 1: Classical geometric scaling era (1997-2004)

Era 2: Equivalent scaling era (2005 – 2016)

Era 3: Hyper-scaling era (2017 – beyond)

ASCENT Center

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Theme 1 Vertical CMOS	Theme 2 Beyond CMOS	Theme 3 Heterogeneous Integration Fabric	Theme 4 Merged Logic-Memory Fabric
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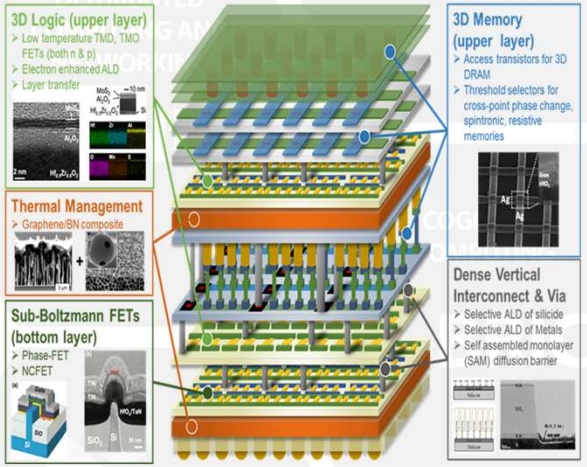
Vertical CMOS
Enable hyper scaling by stacking logic and memory layers in the vertical dimension with ultra-dense connectivity

Beyond CMOS
Combine logic and memory functions and operate spintronic units near thermodynamic limit

Multi-function Heterogeneous Fabric
Combine the best of chip technologies and design IPs into a heterogeneous microsystem by tiling dielets together on an ultra-dense and energy-efficient interconnect fabric

Merged Logic-Memory Fabric
Leverage innovations in vertical 3D memory technologies to create merged logic-memory fabrics to accelerate cognitive and secure computing workloads

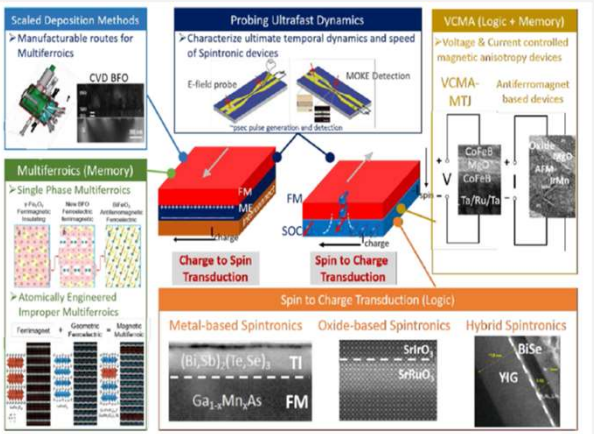
Theme 1: Vertical CMOS



Why Vertical CMOS:
Reduce interconnect bottleneck and increase # gates/mm².

Challenges:
Protect bottom layer transistors, align top layer with bottom layer, low resistivity inter-layer vias, thermal management, and cost of layering logic and memory in a single die.

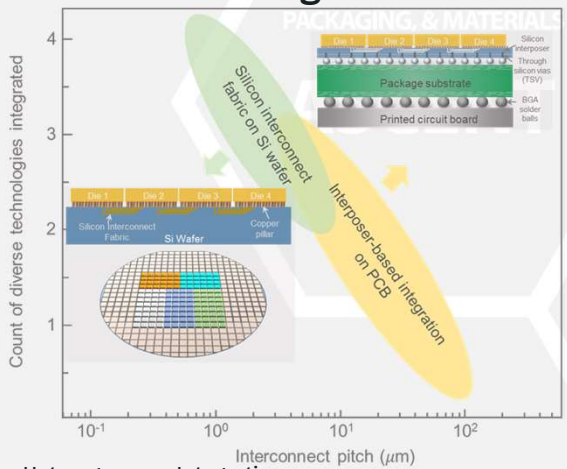
Theme 2: Beyond CMOS



Why Beyond CMOS:
Non-volatile, ultra-high speed, unlimited endurance, energy dissipation approaching thermodynamic limit.

Challenges:
Low voltage (100mV) driven manipulation of magnetic information, convert magnetic information into voltage signal of 100mV, switch magnetic order at 10s of picosecond, and low current driven manipulation of magnetic memory.

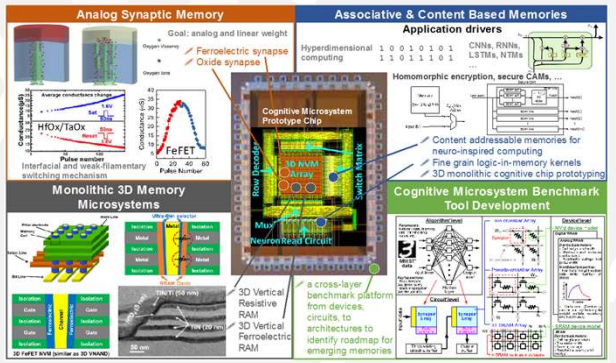
Theme 3: Heterogeneous CMOS



Why Heterogeneous Integration:
PCB ultimately limits size, weight, area, performance of microsystems, and silicon IP reuse.

Challenges:
Fine pitch interconnect, micro-aligned integration of functionally, technologically diverse ICs on a universal substrate, reach 2um interconnect spacing and <50 um die to die spacing, and achieve aggregate data transfer rate of 1Tb/s/mm at < 0.1pJ/bit.

Theme 4: Merged Memory Logic



Why Merged Memory Logic Fabric:
Data centric workloads are limited by memory access and memory density.

Challenges:
Synaptic memory with multiple discrete and non-volatile conductance states that are linearly tunable using consecutive voltage pulses, associative and content based memories with built-in local compute features, cross-layer benchmarking platform to evaluate emerging neuromorphic devices and circuits

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