Summit Map

Hardware for Next-Generation Artificial Intelligence (AI) Workshop & Poster Sessions will be held on the Mezzanine Level

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Shuttle Schedule
Departures from Summit Hotels
Monday............................................................1:00 PM
Tuesday...........................................................6:45 AM
Wednesday......................................................6:45 AM

Departures from Palace of Fine Arts
Monday............................................................7:15 PM
Tuesday...........................................................6:15 PM
Wednesday......................................................7:00 PM

(Fairmont San Francisco, Hilton Financial District)

ERI Summit WiFi
Name: ERISummit
Pass: DARPA2018
Welcome to the Electronics Resurgence Initiative Summit

In 1965, the legendary technology pioneer Gordon Moore set us on a 50-year odyssey so consequential that it is defensible to think of our times as the “Microelectronics Age.” In a paper published that year in *Electronics* magazine entitled “Cramming more components onto integrated circuits,” Moore predicted a trajectory of progress in which the transistor count of integrated circuits would roughly double every two years while the cost per transistor would decrease. When the short paper was first published in this niche trade magazine, early readers couldn’t possibly have imagined the impact it would have on the electronics industry. However, from these humble beginnings emerged the line of progress that we today know as Moore’s Law.

The drive to keep Moore’s Law valid has been a defining vector for America’s position of global leadership. The gains that came as electronics technology sprinted forward according to Moore’s Law were not guaranteed but realized through ingenuity and close collaboration between the commercial sector, academia, and government. Today, however, the rising cost of designing integrated circuits, increasing foreign investments, and the commodification of hardware threaten the future health of an innovative and dynamic, domestic, microelectronics community.

DARPA, like so many other research institutions, has turned to Moore’s Law as a means of charting a continued path forward in electronics innovation. For decades, the Agency has invested heavily in the advancement of electronics, yielding many industry-changing technologies while fulfilling Moore’s prophecy.

Since its inception, DARPA has often relied on an open research model that involves pairing with non-defense oriented partners. In contrast to relying on secrecy, as is often required in military research, the investments the Agency has made in the fundamentals of semiconductors under this inclusive and collaborative model have allowed the country to take the lead in pioneering this technology. As we confront the headwinds that face the industry, we once again turn to the open research model to deliver the needed technological advancements that will support our economy and national defense for years to come.

Our Electronics Resurgence Initiative (ERI) builds on this long tradition of successful government-industry partnerships to foster the environment needed for the next wave of U.S. semiconductor innovation. At this critical juncture, we know that both challenges and opportunities lie before the community. We are encouraged by the enthusiasm for this Initiative and the opportunity to collaborate on the path forward. Over the next three days, we hope you will take advantage of all the ERI Summit has to offer – from forging new partnerships to gathering novel insights and contributing to the future evolution of the industry.

Here’s to a specialized, secure, and heavily automated electronics industry.

Dr. William Chappell

Director, Microsystems Technology Office (MTO)
DARPA Electronics Resurgence Initiative

On June 1, 2017, MTO announced its Electronics Resurgence Initiative (ERI) to ensure far-reaching improvements in electronics performance well beyond the limits of traditional scaling. Recognizing challenges to keeping on pace with Moore's Law, ERI draws both on new ("Page 3") and existing ("Foundational") DARPA programs to make a significant investment into enabling circuit specialization and managing complexity. Page three of Gordon Moore's seminal 1965 paper described research areas required to manage the technical and economic challenges we face. In deference to Moore's ideas, ERI's "Page 3" investments support research and development in each of these areas: Architectures, Designs, and Materials and Integration. To fully unlock microelectronics innovation and maintain technical superiority for the Department of Defense (DoD), ERI builds on the tradition of other successful government-industry partnerships and aims to forge forward-looking collaborations among the commercial electronics community, defense industrial base, university researchers, and DoD. DARPA program managers are leading the way with a portfolio of programs specific to ERI and to the applications that will drive next generation electronics:

Mr. Kerry Bernstein
Supply Chain Hardware Integrity for Electronics Defense (SHIELD)

Dr. Young-Kai Chen
Foundations Required for Novel Compute (FRANC)

Dr. Whitney Mason
Reconfigurable Imaging (Relmagine)

Mr. Andreas Olofsson
Posh Open Source Hardware (POSH)
Intelligent Design of Electronic Assets (IDEA)
Common Heterogeneous Integration and IP Reuse Strategies (CHIPS)

Dr. Roy (Troy) Olsson
Near Zero Power RF and Sensor Operations (N-ZERO)

Dr. Tom Rondeau
Domain-Specific System on Chip (DSSOC)

Dr. Linton Salmon
Three Dimensional Monolithic System-on-a-Chip (3DSoC)
System Security Integrated Through Hardware and Firmware (SSITH)
Circuit Realization At Faster Timescales (CRAFT)
Joint University Microelectronics Program (JUMP)

Dr. Hava Siegelmann
Lifelong Learning Machines (L2M)

Mr. Wade Shen
Hierarchical Identify Verify Exploit (HIVE)
Software Defined Hardware (SDH)

Mr. Paul Tilghman
Spectrum Collaboration Challenge (SC2)
## Foundational Programs

### Materials & Integration
Can the integration of unconventional materials enhance conventional silicon circuits and continue the progress traditionally associated with scaling?

- **CHIPS** Chips that improve due to new materials rather than relying on scaling

### Designs Thrust
Can we dramatically lower the barriers to modern system-on-chip (SoC) design and unleash a new era of circuit and system specialization and innovation?

- **CRAFT** Chips that are as easy to create as writing software

### Architectures Thrust
Can we enjoy the benefits of specialized circuitry while still relying on general programming constructs through the proper software/hardware co-design?

- **HIVE** Chips that traverse large-scale sparse graphs

### Driving Applications
Discover the applications that will determine the next generation of electronics.

- **SHIELD** Chips that demonstrate the art of the small
- **N-ZERO** Chips so low power they are almost off
- **ReImagines** Chips that allow for saliency within sensing systems
- **SC2** Smart systems that learn to cooperate
- **L2M** Systems so smart they learn in the field
- **SSITH** Chips with inherent security

### "Page 3" 2018 New Starts

- **FRANC** Chips that improve due to new materials rather than relying on scaling
- **3DSoC** 3D chips that show performance at older nodes
- **POSH** Trustable chips composed of understandable parts
- **IDEA** Chips built from Electronic Design Automation tools that learn
- **SDH** Chips that adapt to dynamic data streams
- **DSSoC** Chips to adapt within defined domains

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"Page 3" 2018 New Starts
# Agenda: Monday, July 23

<table>
<thead>
<tr>
<th>Time</th>
<th>Event</th>
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<tbody>
<tr>
<td>7:30 AM</td>
<td><strong>Workshop Check-In and Breakfast</strong></td>
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<tr>
<td>8:30 AM</td>
<td><strong>ERI “What’s Next” Technical Brainstorming Workshops</strong>&lt;br&gt;Hardware for Next-Generation Artificial Intelligence (AI)&lt;br&gt;Hardware Security&lt;br&gt;Hardware Emulation&lt;br&gt;Integrated Photonics</td>
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<tr>
<td>12:30 PM</td>
<td><strong>Workshops Adjourn</strong>&lt;br&gt;Participants may purchase lunch at nearby locations</td>
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<tr>
<td>1:30 PM</td>
<td><strong>Summit Check-In</strong></td>
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<tr>
<td>2:30 PM</td>
<td><strong>Welcome and Announcement of ERI &quot;Page 3&quot; Selections</strong>&lt;br&gt;Dr. Jay Lewis, Deputy Director, DARPA MTO</td>
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<tr>
<td>3:15 PM</td>
<td><strong>Introduction of Joint University Microelectronics Program (JUMP) Focus Areas</strong>&lt;br&gt;Dr. Linton Salmon, DARPA MTO&lt;br&gt;Dr. Anthony Rowe, Carnegie Mellon University&lt;br&gt;Dr. Valeria Bertacco, University of Michigan&lt;br&gt;Dr. Suman Datta, University Notre Dame&lt;br&gt;Dr. Kaushik Roy, Purdue University&lt;br&gt;Dr. Mark Rodwell, University of California, Santa Barbara&lt;br&gt;Dr. Tajana Rosing, University of California, San Diego</td>
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<tr>
<td>4:30 PM</td>
<td><strong>Keynote: Another Brick in the Wall</strong>&lt;br&gt;Dr. Erica Fuchs, Professor of Engineering and Public Policy, Carnegie Mellon University</td>
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<tr>
<td>5:00 PM</td>
<td><strong>Keynote: New Commercial DoD Partnership Models</strong>&lt;br&gt;Mr. Tom Beckley, Cadence Design Systems</td>
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<td>5:30 PM</td>
<td><strong>Reception and Networking</strong></td>
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<tr>
<td>7:00 PM</td>
<td><strong>Adjourn</strong>&lt;br&gt;*Shuttles depart to Summit hotels (Fairmont San Francisco, Hilton Financial District) promptly at 7:15pm</td>
</tr>
</tbody>
</table>
ERI "Page 3" Selections

Materials & Integration Thrust

**3DSoC**
Georgia Institute of Technology
Massachusetts Institute of Technology

**FRANC**
Applied Materials
Ferric
HRL Laboratories
University of California, Los Angeles
University of Illinois at Urbana–Champaign
University of Minnesota

Architectures Thrust

**DSSOC**
Arizona State University
IBM
Oak Ridge National Laboratory
Stanford University

**SDH**
Georgia Institute of Technology
Intel
NVIDIA
Princeton University
Qualcomm
Stanford University
Systems & Technology Research
University of Michigan
University of Washington

Designs Thrust

**POSH**
Brown University
LeWiz
Princeton University
Sandia National Labs
Stanford University
Synopsys
University of Southern California
University of Utah
University of Washington
Xilinx

**IDEA**
Cadence Design Systems
Northrop Grumman
Princeton University
Purdue University
University of California, San Diego
University of Illinois at Urbana–Champaign
University of Michigan
University of Minnesota
University of Utah
University of Texas at Austin
Yale University
# Agenda: Tuesday, July 24

<table>
<thead>
<tr>
<th>Time</th>
<th>Session</th>
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<tbody>
<tr>
<td>7:00 AM</td>
<td><strong>Check-In and Breakfast</strong></td>
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<tr>
<td>8:00 AM</td>
<td><strong>Opening Remarks and Introduction</strong></td>
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<td></td>
<td>Dr. William Chappell, Director, DARPA MTO</td>
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<tr>
<td>8:05 AM</td>
<td><strong>Plenary: The End of Moore’s Law &amp; Faster General Purpose Computing, and a New Golden Age</strong></td>
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<td>Dr. John Hennessy, Chairman, Alphabet</td>
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<td>8:50 AM</td>
<td><strong>Keynote: The DARPA Mission</strong></td>
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<td>Dr. Steven Walker, Director, DARPA</td>
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<td>9:05 AM</td>
<td><strong>The Intertwined History of DARPA &amp; Moore’s Law</strong></td>
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<td></td>
<td>Dr. William Chappell, Director, DARPA MTO</td>
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<tr>
<td>9:35 AM</td>
<td><strong>Break</strong></td>
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<tr>
<td>10:00 AM</td>
<td><strong>Keynote: The Future is So Bright - the Era of Heterogeneous Compute</strong></td>
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<td>Dr. Mike Mayberry, CTO, Intel</td>
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<tr>
<td>10:30 AM</td>
<td><strong>Common Heterogeneous Integration and IP Reuse Strategies (CHIPS)</strong></td>
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<td></td>
<td>Mr. Andreas Olofsson, DARPA MTO</td>
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<td>Mr. Sergey Shumaryev, Intel</td>
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<td>Mr. Craig Hornbuckle, Jariet Technologies</td>
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<td>Mr. Richard Kingdon, Micross</td>
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<tr>
<td>11:15 AM</td>
<td>&quot;Page 3&quot; - Three Dimensional Monolithic System-on-a-Chip (3DSoC)</td>
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<td></td>
<td>Dr. Linton Salmon, DARPA MTO</td>
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<td>Dr. Max Shulaker, Massachusetts Institute of Technology</td>
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<td>Dr. Subhasish Mitra, Stanford University</td>
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<td>12:00 PM</td>
<td><strong>Keynote: Navigating the Perfect Storm - Enabling the A.I. Era</strong></td>
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<td>Mr. Gary Dickerson, CEO, Applied Materials</td>
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"It may prove to be more economical to build large systems out of smaller functions, which are separately packaged and interconnected."

—Gordon Moore, 1965
### Agenda: Tuesday, July 24

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<tr>
<th>Time</th>
<th>Event</th>
<th>Details</th>
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<tbody>
<tr>
<td>12:30 PM</td>
<td>&quot;Page 3&quot; – Foundations Required for Novel Compute (FRANC)</td>
<td>Dr. Young-Kai Chen, DARPA MTO</td>
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<td>Mr. Steve Pawlowski, Micron</td>
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<td>Dr. Naresh Shanbhag, University of Illinois Urbana-Champaign</td>
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<tr>
<td>1:15 PM</td>
<td>Lunch</td>
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<tr>
<td>2:30 PM</td>
<td>Keynote: At the Heart of Impact</td>
<td>Dr. Aart de Geus, Co-CEO &amp; Chairman, Synopsys</td>
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<tr>
<td>3:00 PM</td>
<td>Circuit Realization At Faster Timescales (CRAFT)</td>
<td>Dr. Linton Salmon, DARPA MTO</td>
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<td>Dr. Elad Alon, University of California, Berkeley</td>
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<td>Dr. Brucek Khailany, Director, ASIC &amp; VLSI Research, NVIDIA</td>
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<tr>
<td>3:45 PM</td>
<td>&quot;Page 3&quot; – Intelligent Design of Electronic Assets (IDEA) &amp; Posh Open Source Hardware (POSH)</td>
<td>Mr. Andreas Olofsson, DARPA MTO</td>
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<td>Dr. David White, Cadence Design Systems</td>
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<td>Dr. Andrew Kahng, University of California, San Diego</td>
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<td>Dr. Clark Barrett, Stanford University</td>
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<td>Mr. Peter Ryser, Xilinx</td>
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<td>Mr. Christopher Tice, Synopsys</td>
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<td>5:15 PM</td>
<td>Broader Defense Department Technology Directions</td>
<td>Ms. Kristen Baldwin, Acting Deputy Assistant Secretary of Defense for Systems Engineering</td>
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<tr>
<td>5:30 PM</td>
<td>Adjourn</td>
<td>*Shuttles depart to Summit hotels (Fairmont San Francisco, Hilton Financial District) promptly at 6:15pm</td>
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</tbody>
</table>

"Perhaps newly devised design automation procedures could translate from logic diagram to technological realization with any special engineering.”
—Gordon Moore, 1965
Agenda: Wednesday, July 25

7:00 AM  Check-In and Breakfast

7:30 AM  Networking and Poster Session

Architectures Thrust

“we could amortize the engineering over several identical items, or evolve flexible techniques for the engineering of large functions so that no disproportionate expense need be borne by a particular array.”
—Gordon Moore, 1965

9:30 AM  Keynote: The Accelerator Age
Dr. Bill Dally, Chief Scientist & Senior Vice President, NVIDIA

10:00 AM  Hierarchical Identify Verify Exploit (HIVE)
Mr. Wade Shen, DARPA Information Innovation Office (I2O)
Dr. Joshua Fryman, Intel
Dr. Shekhar Borkar, Qualcomm

10:30 AM  "Page 3" – Software Defined Hardware (SDH)
Mr. Wade Shen, DARPA I2O
Dr. Luca Carloni, Columbia University
Dr. Suresh Jagannathan, Purdue University

11:00 AM  "Page 3" – Domain-Specific System on Chip (DSSoC)
Dr. Tom Rondeau, DARPA MTO
Dr. Pradip Bose, IBM
Dr. Dan Bliss, Arizona State University

12:00 PM  Lunch

Driving Applications

1:15 PM  Keynote: Next Wave of Electronics-Driven Applications
Dr. Walden Rhines, CEO, Mentor Graphics

1:45 PM  Applications|Sensors – Near Zero Power RF and Sensor Operations (N-ZERO)
Dr. Troy Olsson, DARPA MTO
Dr. Dennis Sylvester, University of Michigan
**Agenda: Wednesday, July 25**

<table>
<thead>
<tr>
<th>Time</th>
<th>Session</th>
<th>Speakers</th>
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<tr>
<td>2:15 PM</td>
<td>**Applications</td>
<td>Sensors – Reconfigurable Imaging (ReImagine)**</td>
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<td></td>
<td>Dr. Whitney Mason, DARPA MTO</td>
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<td>Dr. Peter Grossman, MIT Lincoln Laboratory</td>
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<td>Dr. Saibal Mukhopadhyay, Georgia Institute of Technology</td>
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<td>2:45 PM</td>
<td>Break</td>
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<tr>
<td>3:15 PM</td>
<td>**Applications</td>
<td>Security – System Security Integrated Through Hardware and Firmware (SSITH)**</td>
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<td></td>
<td>Dr. Linton Salmon, DARPA MTO</td>
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<td>Dr. Joseph Kiniry, Galois</td>
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<td>3:45 PM</td>
<td>**Applications</td>
<td>Security – Supply Chain Hardware Integrity for Electronics Defense (SHIELD)**</td>
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<td></td>
<td>Mr. Kerry Bernstein, DARPA MTO</td>
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<td>Dr. Michael Kane, SRI International</td>
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<td>Dr. Christopher Lantman, SRI International</td>
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<td>4:15 PM</td>
<td>**Applications</td>
<td>Learning – Spectrum Collaboration Challenge (SC2)**</td>
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<td>Mr. Paul Tilghman, DARPA MTO</td>
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<td>Dr. Greg Wright, Nokia Bell Labs</td>
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<td>4:45 PM</td>
<td>**Applications</td>
<td>Learning – Lifelong Learning Machines (L2M)**</td>
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<td>Dr. Hava Siegelmann, DARPA I2O</td>
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<td>Dr. Hod Lipson, Columbia University</td>
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<td>5:15 PM</td>
<td>Where Do We Go From Here?</td>
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<td>DARPA Program Managers will discuss the challenges and opportunities facing future technologies with an outbrief on the Workshops and Summit</td>
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<td>6:15 PM</td>
<td>Adjourn</td>
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<td>*Shuttles depart to Summit hotels (Fairmont San Francisco, Hilton Financial District) promptly at 7:00pm</td>
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**Materials and Integration Thrust**

Scalable, Energy-Efficient, And High-Throughput All-Memristor Neuromorphic Processor
Spintronic Stochastic Dataflow Computing
MRAM-based Deep In-memory Architectures
A Synaptic Switch for Neuromorphic Compute
Advanced Magnetic Tunnel Junctions for Computation in and Near Random Access Memory
Heterogeneous Integration Enables Next Generation Systems
2.5D System Design Using Modular Chiplets Based on Standard Interface
Low-Cost, Fast-Turn Advanced Microelectronic Systems for the DoD
Enabling the Digital Microwave Revolution: Quad-Channel Digital RF Transceiver Chiplet
Synopsis Semiconductor IP in Chiplet Format with AIB Interface for CHIPS Integration
3DSoC: Transforming Ideas to Reality
RTL-to-GDS Tools and Methodologies for Sequential Integration Monolithic 3D ICs

**Architectures Thrust**

Embedded AI for Autonomous Vehicles: Efficient Programmability of Cognitive Heterogeneous Systems (EPOCHS)
Development Framework for Next Generation High-Performance Processors
Agile Hardware: Rethinking DSSoC Design
Enabling Co-Design for DSSoC Processors
Plasticine: A Universal Data Analytics Accelerator
Transmuter – A Reconfigurable Computer
Dynamic, Data-Aware Reconfiguration
Future Graph Analytics
Unprecedented Efficient Graph Analytics
A Software Toolkit for Accelerating Graph Algorithms
A Hybrid Attributed Generic Graph Library Environment

**Participant**

<table>
<thead>
<tr>
<th>MTO Program</th>
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<tbody>
<tr>
<td>HRL Laboratories</td>
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<tr>
<td>University of California, Los Angeles</td>
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<td>University of Illinois Urbana-Champaign</td>
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<td>Applied Materials</td>
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<td>Synopsis</td>
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<td>Massachusetts Institute of Technology</td>
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<td>Georgia Institute of Technology</td>
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<td>Georgia Institute of Technology</td>
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<td>Pacific Northwest National Laboratory</td>
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Designs Thrust

OpenROAD: Foundations and Realization of Open, Accessible Design
Generative User Intent Design of Electronics (GUIDE)
Fully-Autonomous SoC Synthesis using Customizable Cell-Based Synthesizable Analog Circuits
CoSA: Integrated Open-Source Formal Verification
QED Bug Detection and Localization
AMS Verification Technologies and Flow for Enabling POSH SoCs
Mixed-Signal SoC Emulation Technology
Agile Hardware Design in Extreme Process Technologies (AHDEPT)
Modular Approach to Circuits and Hardware (MATCH)

Driving Applications

A microscopic RF Authentication IC for Preventing Counterfeit Electronics
Microscopic Taggant Technology Protecting the DoD Supply Chain from Counterfeit Electronics
Physical anti-tamper protection and passive sensor technologies
RF and Acoustic methods for Power & Communication
Wireless Power Transfer and Communication to a Miniature Sensing RFID for Defense
Modular Optical Aperture Building Blocks
Integrated Photonics for Multi-Tbps I/O
Enabling 3D Technology
Sub-10µm Pitch 3D Integration Technology for Adaptive Focal Plane Array Imagers
CAMEL: Camera Adaptation with Embedded Machine Learning Based Feedback Control
Sensing Infrared Without Power
MONO: A sub-threshold microcontroller for near-zero-power sensor applications
Asleep Yet Aware, Awake on Declare Virginia Efficient Near-zero Ultra-low-power System
Near-Zero Power Wake-up Receivers
SSIITH: TA1 (Hardware) Performers
SSIITH: System Security Integrated Through Hardware and Firmware
Lifelong learning of perception and action in autonomous systems
Designing adaptive systems that dynamically reprogram themselves based on context
Dynamically revising neural networks via continual knowledge feedback
Self-directed lifelong visual learning
Hippocampal indexing and cortical hierarchies: the drivers of quasi-continuous learning
Spectrum Collaboration Challenge Overview
SC2 PE1 Results
Colosseum RF Testbed
High Bandwidth Phase-Change Switch Technology
Heterogeneous Integration and Cooling for 2.5D and 3D Circuits

Joint University Microelectronics Program

Computing On Network Infrastructure for Pervasive Perception, Cognition, and Action(ConIX)
Center for Brain-inspired Computing Enabling Autonomous Intelligence (C-BRIC)
Center for Converged Terahertz Communications and Sensing (ComSecTer)
Applications Driving Architectures (ADA) Center
Applications and Systems driven Center for Energy-Efficient Integrated Nanotechnologies (ASCENT)
Center for Research on Intelligent Storage and Processing-in-memory (CRISP)

Participant | MTO Program
--- | ---
University of California, San Diego | IDEA
Cadence Design Systems | IDEA
Northrop Grumman/JITx | IDEA
University of Michigan | IDEA
Stanford University | POSH
Stanford University | POSH
Sandia | POSH
Synopsys | POSH
University of California, Berkeley | CRAFT
NVIDIA | CRAFT

Participant | MTO Program
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SRI International | SHIELD
Northrop Grumman | SHIELD
The Charles Stark Draper Laboratory | SHIELD
University of Illinois Urbana-Champaign | SHIELD
University of California, Berkeley | SHIELD
Analog Photonics | MOABB
Ayar Labs | Resulted from POEM
Nhanced | Relimagine
Micross | Relimagine
Georgia Institute of Technology | Relimagine
Northeastern University | N-ZERO
ARM | N-ZERO
University of Virginia | N-ZERO
University of California, San Diego | N-ZERO
Galois Inc | SSITH
DARPA | SSITH
University of Pennsylvania | L2M
Argonne National Laboratory | L2M
University of North Carolina at Chapel Hill | L2M
Toyota Technological Institute at Chicago | L2M
University of California San Diego | L2M
DARPA | SC2
DARPA | SC2
DARPA | SC2
HRL Laboratories | Resulted from RF FPGA
Georgia Institute of Technology | ICECool

Participant | MTO Program
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Carnegie Mellon University | JUMP
Purdue University | JUMP
University of California, San Diego | JUMP
University of Michigan | JUMP
University Notre Dame | JUMP
University of Virginia | JUMP
Since its inception, DARPA has supported projects in the electronics space. With ERI, we are concentrating on the electronics sector more than ever. MTO believes that an initiative is important to emphasize the connectivity between many different programs. Teaming between programs is where a lot of innovation can happen.